Architecture at the End of Moore

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In this work we examine the evolution of architectural features at the end of silicon scaling. In particular, we will expand on power constraints and Dark Silicon, i.e., the inability of keeping all of the cores active under power constraints [1]; reliability issues that will render our architectures stochastic [2], and power-efficiency in relation to the still growing Memory-Wall problem [3,4]. We will discuss the current trends in computer architecture, in particular the trend towards heterogeneous architectures [5] and how this might affect interfacing with novel devices. While CMOS-based computing is here to stay for quite some time after the end of Moore's law, we will attempt to surmise in what respect novel devices can integrate with CMOS and ameliorate some of its problems.

References

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