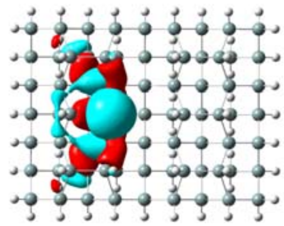
2nd AtMol International Workshop
12 – 13 Jan., 2012

Dangling Bond Logic: Designing Boolean Logic Gates on a Si(100)-H surface



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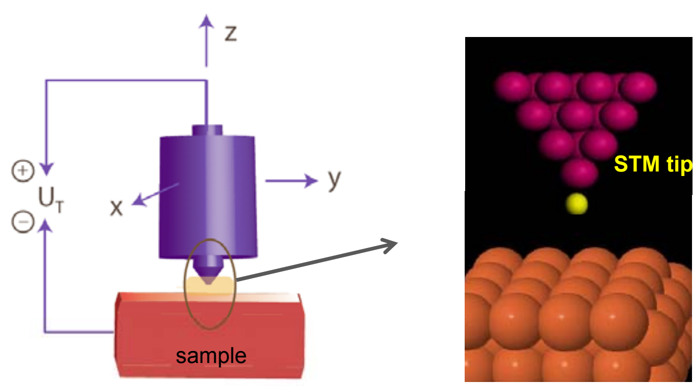
Christian Joachim

Outline

- Dangling Bonds (DBs) on semiconductor surfaces
- H-junction along a Si(100)-(2x1)-H atomic wire
- Boolean DB logic gates on Si(100)-(2x1)-H surface

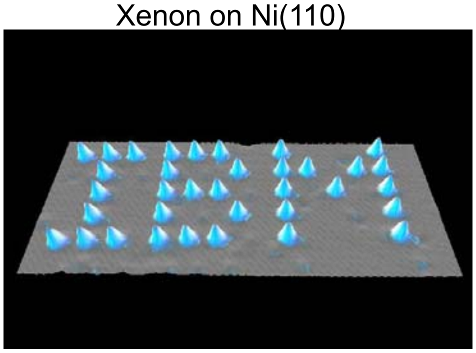
Manipulating single atoms using STM



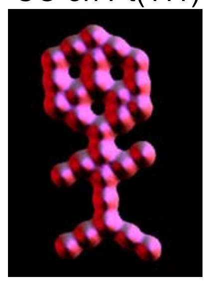
Surface imaging tool based on quantum tunneling
Controllably manipulate atoms on a surface. Eigler, 1989

STM molecular art

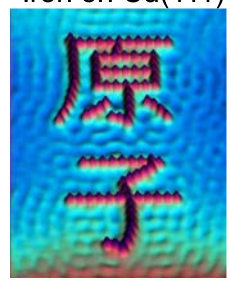
Xenon on Ni(110)



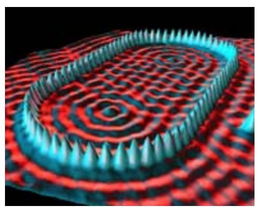
CO on Pt(111)



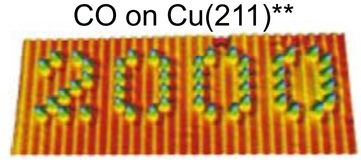
Iron on Cu(111)



Iron on Cu (111)

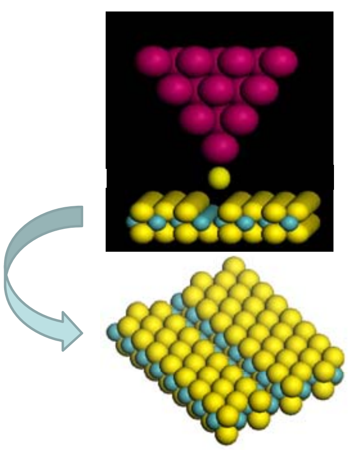


CO on Cu(211)**

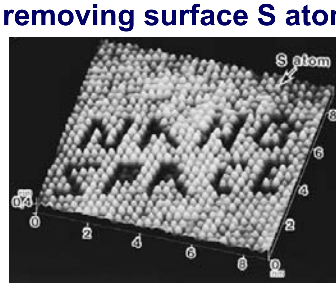


http://www.almaden.ibm.com/vis/stm/atomo.html
Meyer *et al.* *Chem. Phys.* **2, 361 (2001)

Selective removal of atoms with STM on MoS_2



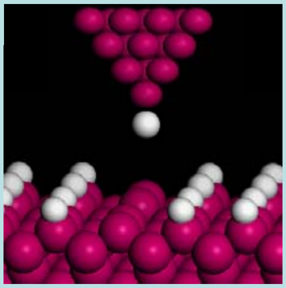
“NANO SPACE” written on MoS_2 by removing surface S atoms



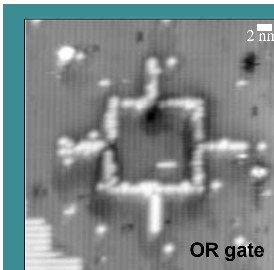
Hosaka *et al.* *J. Vac. Sci. Technol.* 1995

Atomic line formed by removing surface S atoms with an STM tip
The de-passivated sites create dangling bonds (DBs)

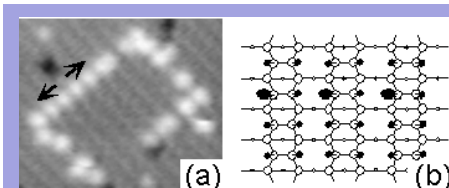
DBs on a Si(100)-(2x1)-H surface



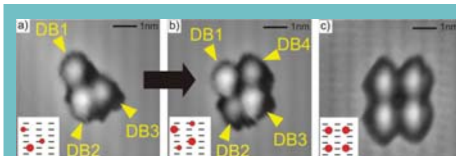
Selective removal of the surface H atoms using STM tip



Soukiassian et al., Surf. Sci. Rev. **528**, 121 (2003)



Hitosugi et al., Appl. Phys. A **66**, S695 (1998)

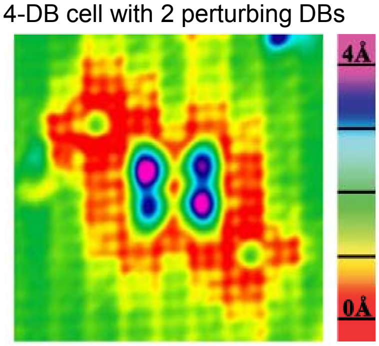


Haider et al., Phys. Rev. Lett. **102**, 046805 (2009)

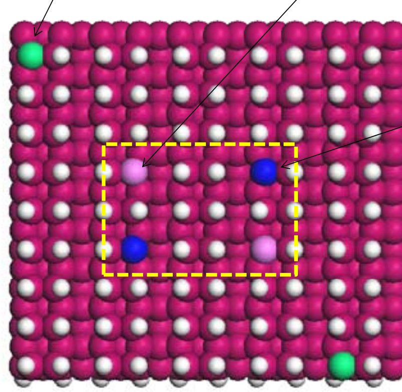
DBs on a Si(100)-(2x1)-H surface

Precise control

STM image of SiH surface with 4-DB cell with 2 perturbing DBs

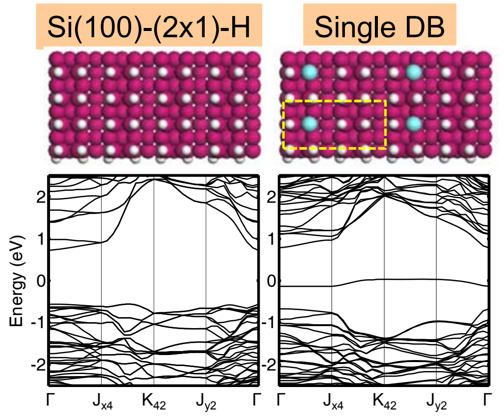


Haider *et al.*, *PRL* 2009



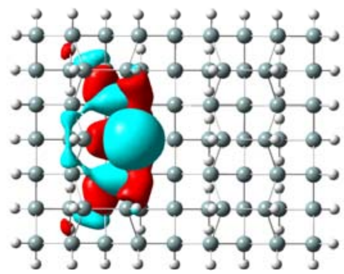
DBs closer to the diagonal perturb DBs

DB state within the Si(100)-(2x1)-H band gap



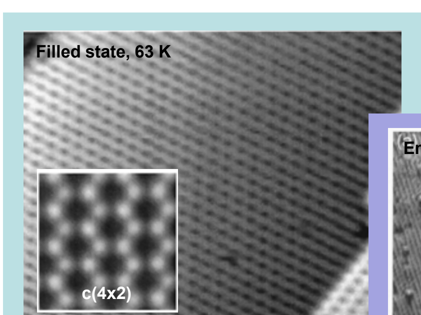
Calculated using VASP (DFT-PBE), 4x2 unit cell, 5 layers

DB orbital image

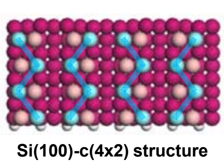


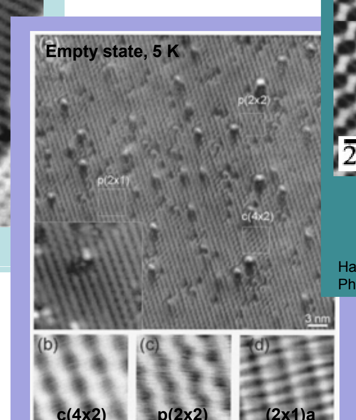
Removing surface H atoms introduces states in the Si(100) surface band gap.
DB states are coupled to subsurface orbitals

STM images of clean Si(100) surface

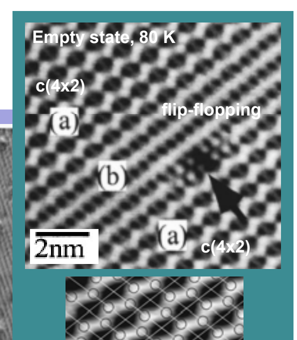


Yokoyama et al.,
Phys. Rev. B **61**, R5078 (2000)



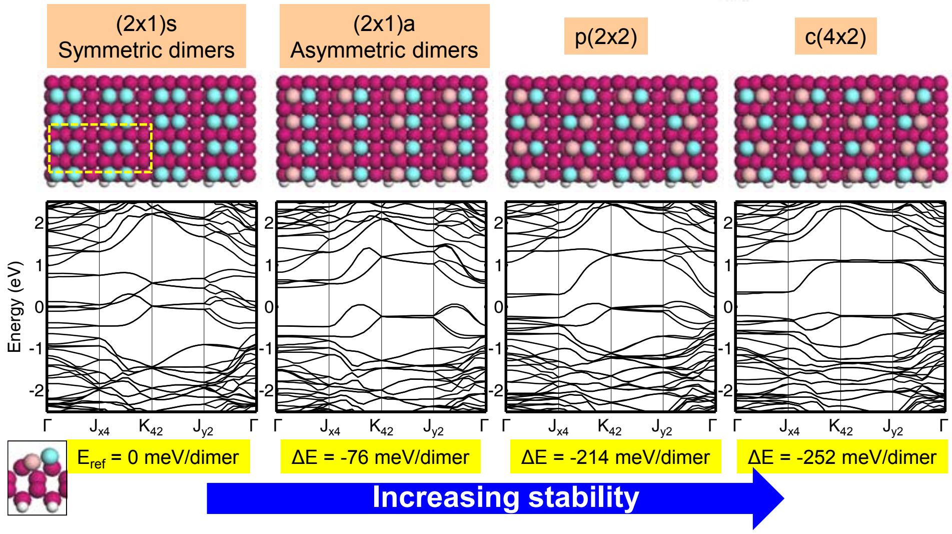


Perdigao et al.,
Phys. Rev. Lett. **92**, 216101 (2004)



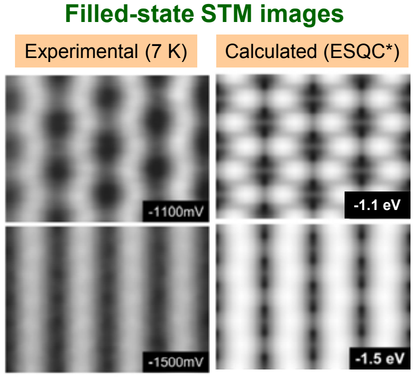
Hata et al.,
Phys. Rev. B **64**, 235310 (2001)

Si(100) surface reconstructions

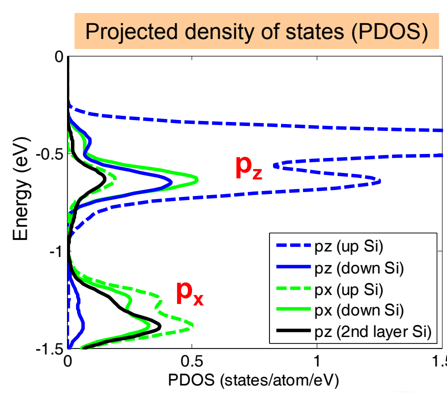


Bias dependence of the STM image of the Si(100)-c(4x2) surface

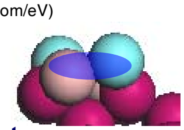
Filled-state STM images



Manzano et al., Phys. Rev. B **83**, 201302 (2011)

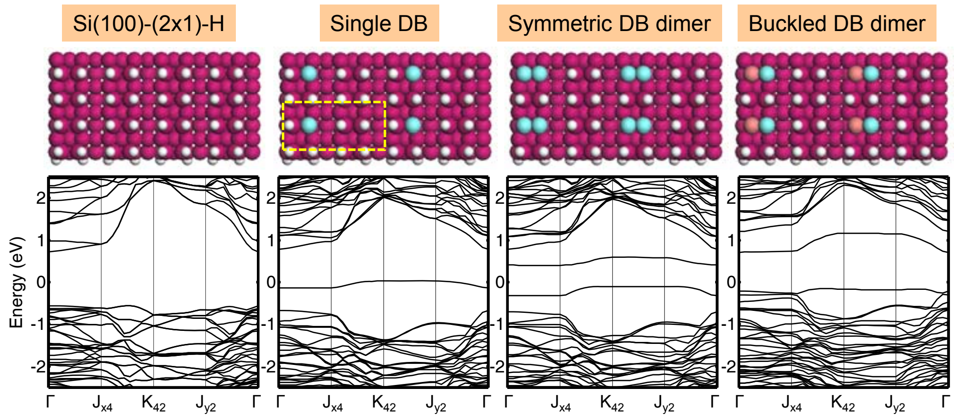


- **STM image and PDOS calculated using an Extended Hückel approximation fitted to DFT-PBE band structure**
- **STM image changes with bias because different states are probed: p_z states dominate at small bias, p_x states dominate at larger bias**



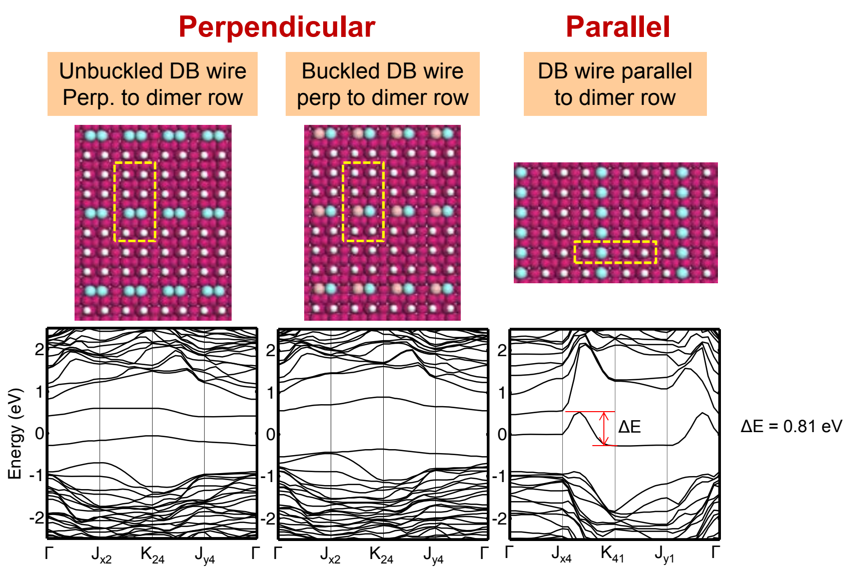
* Sautet et al., Phys. Rev. B **38**, 12238 (1988)

DB states on Si(100)-(2x1)-H



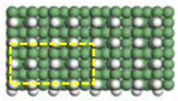
DBs introduce π and π* states in the gap, leading to π and π* bands in a wire

DB wires on Si(100)-(2x1)-H

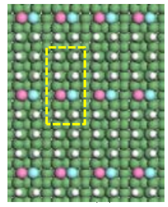


DBs on other semiconductor surfaces: Ge(100)

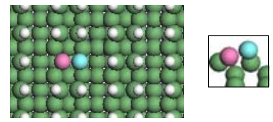
Ge(100)-(2x1)-H

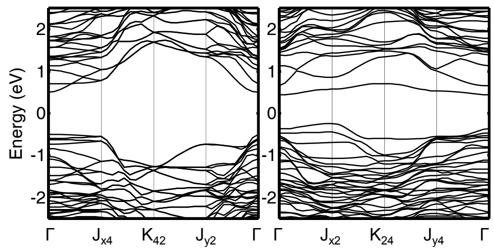


Buckled DB wire perp to dimer row



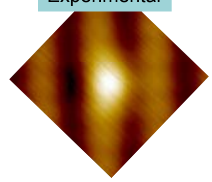
Isolated buckled DB dimer



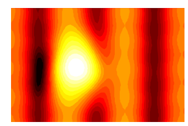


Filled-state STM images

Experimental



Calculated (Green*)

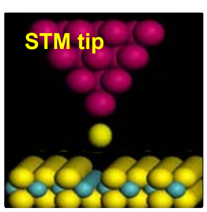


Kolmer et al., paper in prep (AtMol)

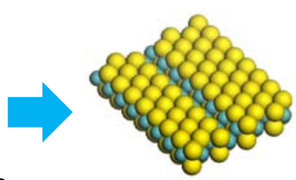
*Green method: Cerda et al., Phys. Rev. B **56**, 15885 (1997)

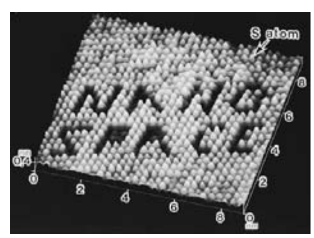
DBs on other semiconductor surfaces: MoS_2

Extraction of S atoms



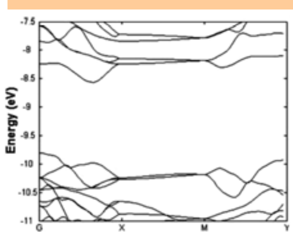
MoS_2



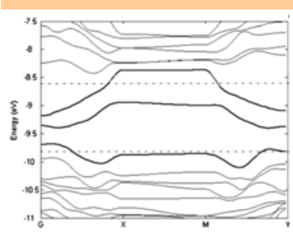


Hosaka et al.,
J. Vac. Sci. Technol B **13**, 2813 (1995)

MoS_2 surface band structure **without** atomic wire



MoS_2 surface band structure **with** atomic wire



Removing an S atom introduces 3 states in the band gap

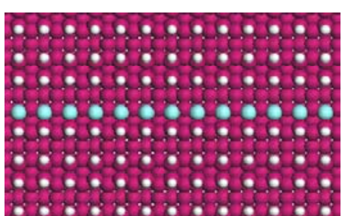
Yong, Otalvaro, Saeys, Joachim, Phys. Rev. B **77**, 205429 (2008)

Outline

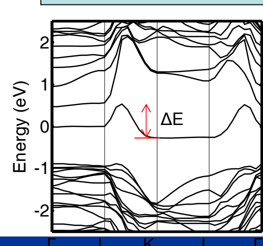
- **Dangling Bonds (DBs) on semiconductor surfaces**
- **H-junction along a Si(100)-(2x1)-H atomic wire**
- **Boolean DB logic gates on Si(100)-(2x1)-H surface**

H-junction along a DB wire

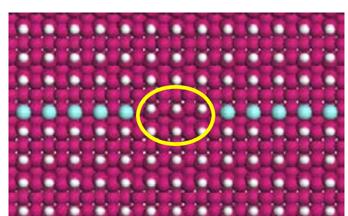
Si(001)-(2x1)-H surface with parallel DB atomic wire



Electron transmission

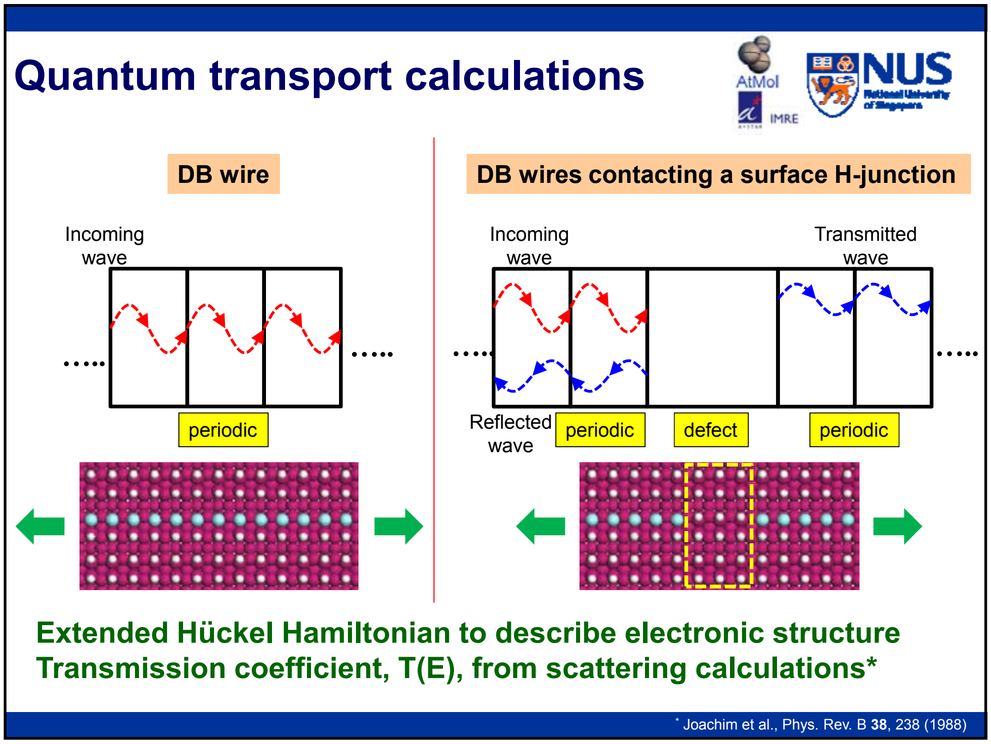


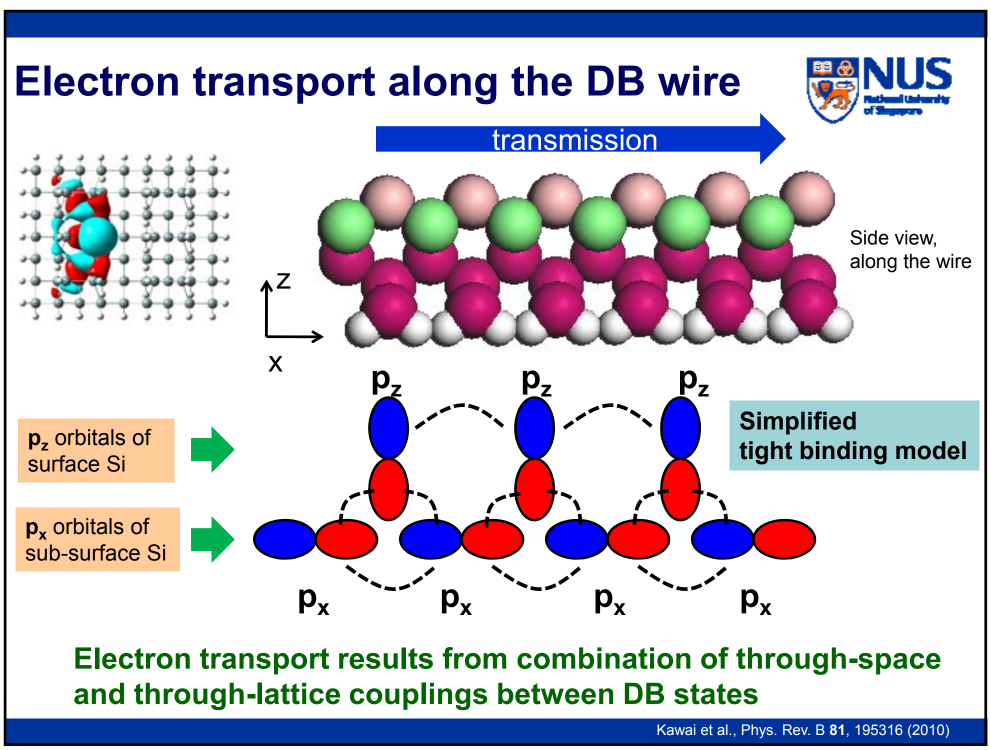
DB atomic wire with hydrogen tunneling junction



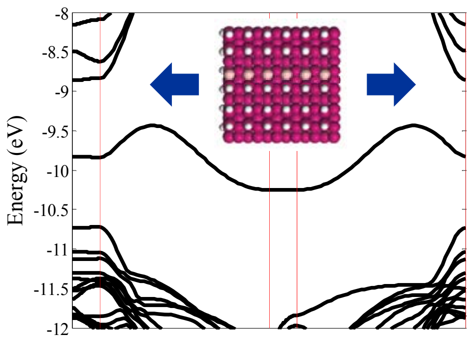
Electron transmission

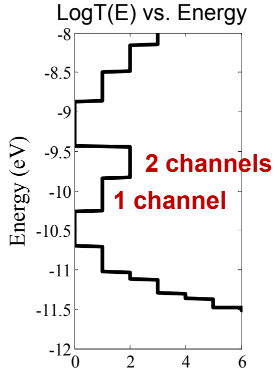
Can a H-junction introduce a tunneling barrier?


Quantum transport calculations
AtMol
IMRE
NUS
National University of Singapore
DB wire
Incoming wave
periodic
DB wires contacting a surface H-junction
Incoming wave
Transmitted wave
Reflected wave
periodic
defect
periodic
Extended Hückel Hamiltonian to describe electronic structure
Transmission coefficient, T(E), from scattering calculations*
* Joachim et al., Phys. Rev. B 38, 238 (1988)


Electron transport along the DB wire
NUS
National University of Singapore
transmission
Side view, along the wire
Z
X
p_z
p_z
p_z
p_z orbitals of surface Si
p_x orbitals of sub-surface Si
Simplified tight binding model
p_x
p_x
p_x
p_x
Electron transport results from combination of through-space and through-lattice couplings between DB states
Kawai et al., Phys. Rev. B 81, 195316 (2010)

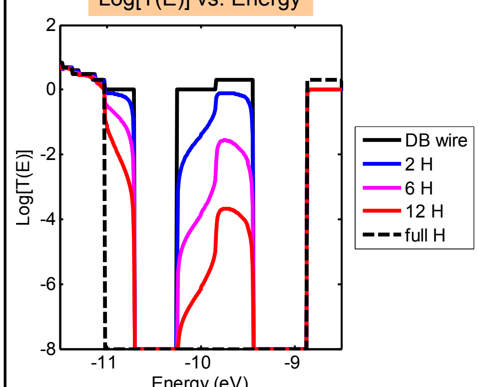
Electron transport along the DB wire

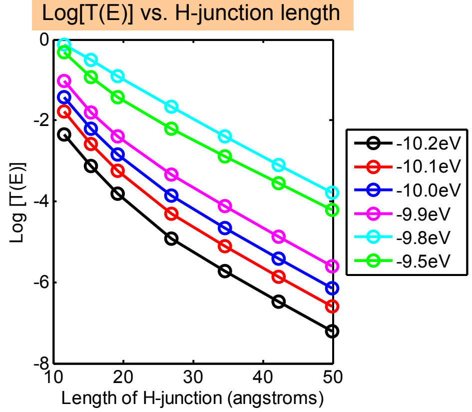




Transmission channels in wire direction within the energy gap
DB wire band has a "2-channel" and "1-channel" region

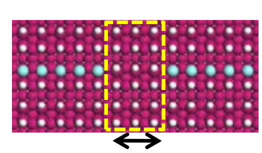
Tunneling through H-junction





T(E) decreases exponentially with H junction length

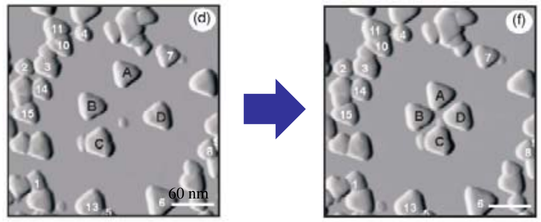
$$T = T_0 e^{-\gamma d}$$ **γ = 0.20 ~ 0.23 Å^{-1}**



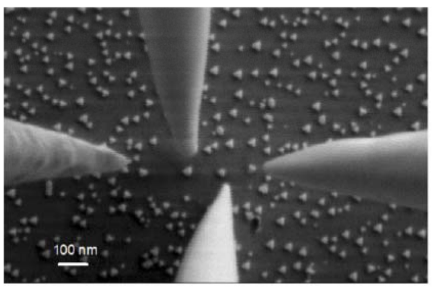
Kawai et al., Phys. Rev. B **81**, 195316 (2010)

Gold islands on MoS_2 surface: Planar metallic contacts

Au nano-islands can be positioned with a UHV-STM on a MoS_2 surface with a 0.5 nm precision



Yang et al., J. Vac. Sci. Technol. B **25**, 1694 (2007)

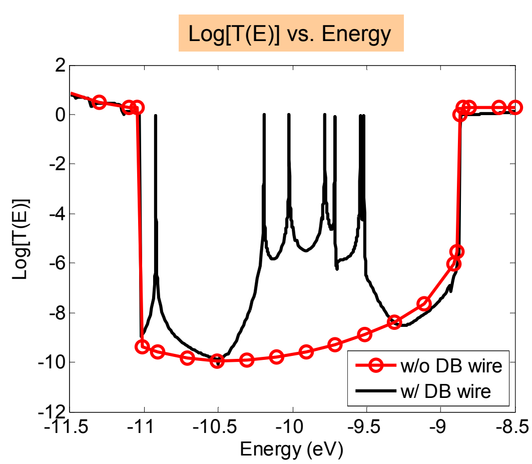


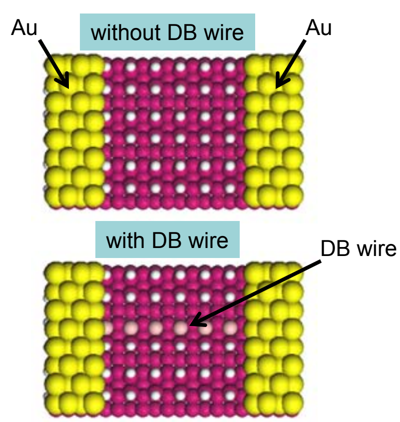
Current-voltage characteristics between two Au nano-islands can be measured with STM probes

Large surface band gap is required to minimize surface leakage currents

Joachim et al., J. Phys.: Condens. Matter 22, 084025 (2010)

Transport along a DB wire contacted by metallic electrodes

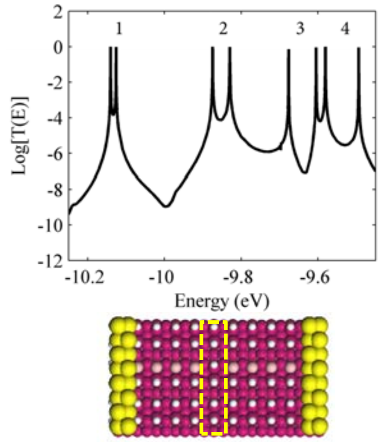




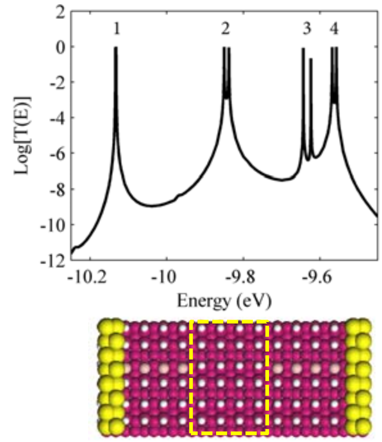
Resonance peaks resulting from the DB states appear within the energy range of the infinite wire band

Tunneling through H-junction connected by a DB wire and metallic electrodes

Log[T(E)] vs. Energy
4DB – 1H – 4DB



Log[T(E)] vs. Energy
4DB – 4H – 4DB

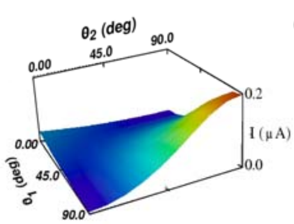


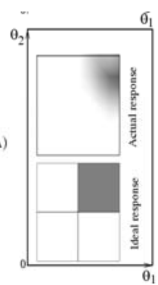
Resonance peaks split, and splitting depends on the coupling through the H junction

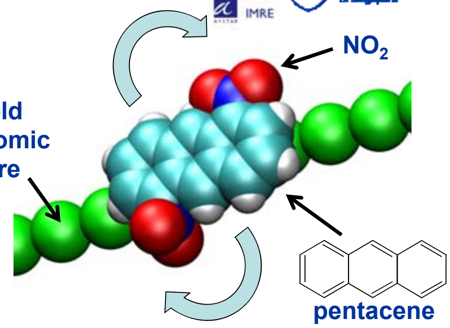
Outline

- **Dangling Bonds (DBs) on semiconductor surfaces**
- **H-junction along a Si(100)-(2x1)-H atomic wire**
- **Boolean DB logic gates on Si(100)-(2x1)-H surface**

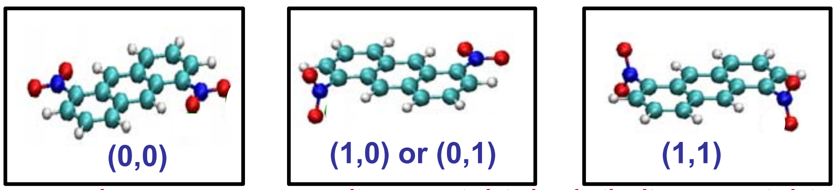
Single molecule logic gates







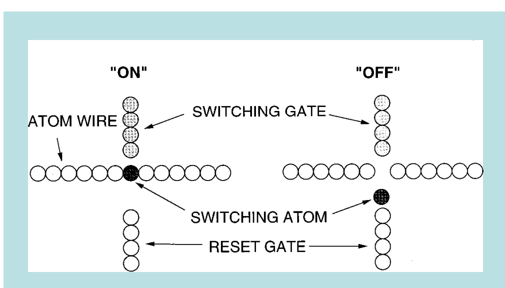
Twisting a nitro group: '0' →'1' logic input

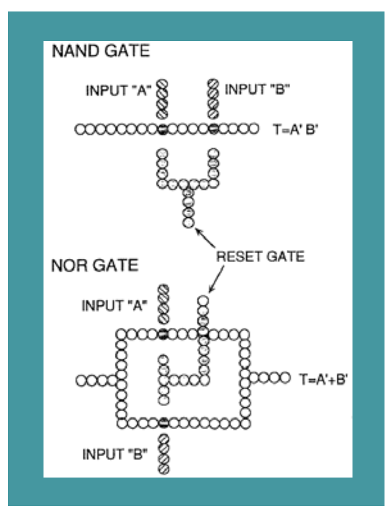


planar | one nitro group twisted | both nitro groups twisted

Renaud, Ito, Shangguan, Saeys, Hliwa, Joachim, Chem Phys Lett, **2009**

Atom switching devices



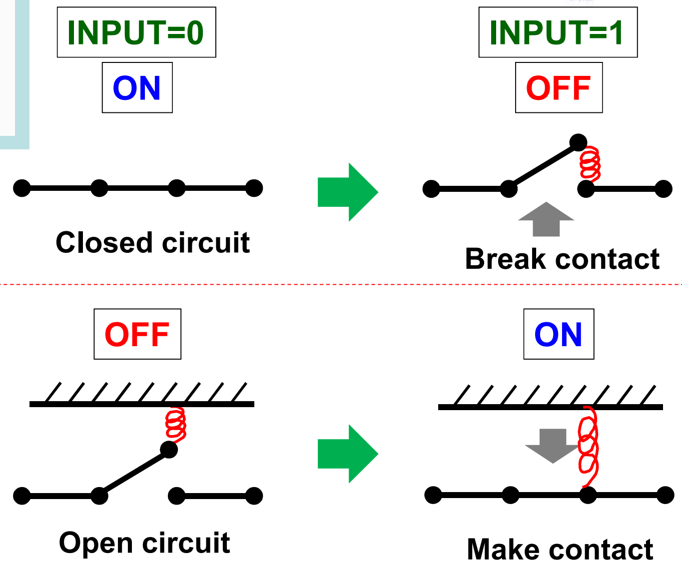


The switching atom is displaced from the atom wire by the electric field from the switching gate

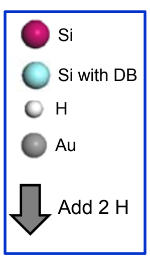
Conceptually, logic circuits can be built using this concept

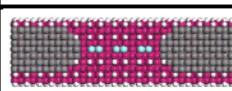
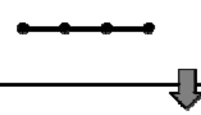
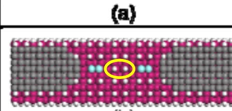
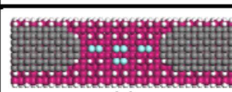
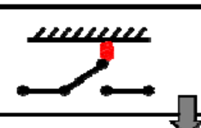
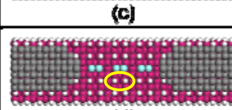
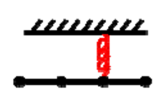
Wada et al., J. Appl. Phys. 74, 7321 (1993)

Classical switch



DB Switches on a Si(100) surface

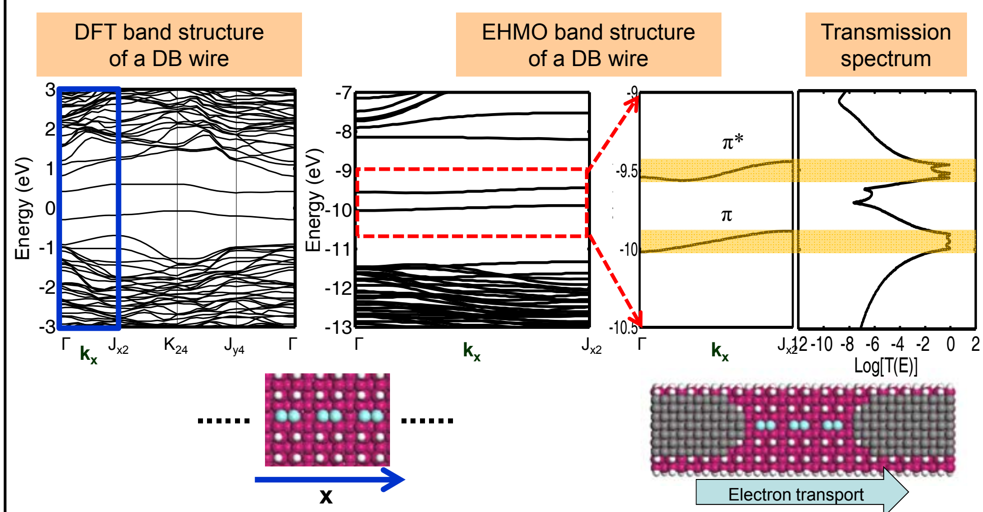


	IN	OUT	Atomic structure	Classical structure
Inverter	0	ON	 (a)	
	1	OFF	 (b)	
Follower	0	OFF	 (c)	
	1	ON	 (d)	

Does this concept work?

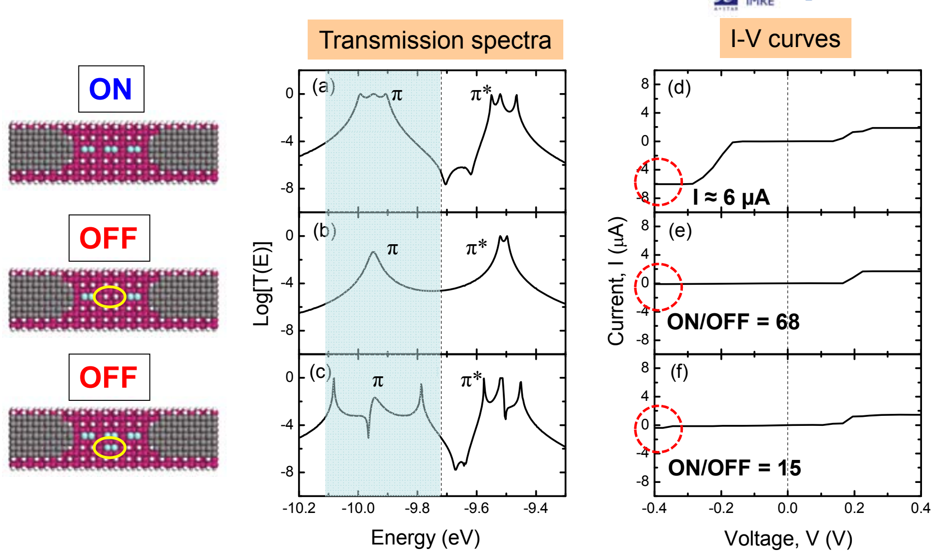
Kawai et al., J. Phys.; Condens. Matter, submitted

Band structure of a perpendicular DB wire

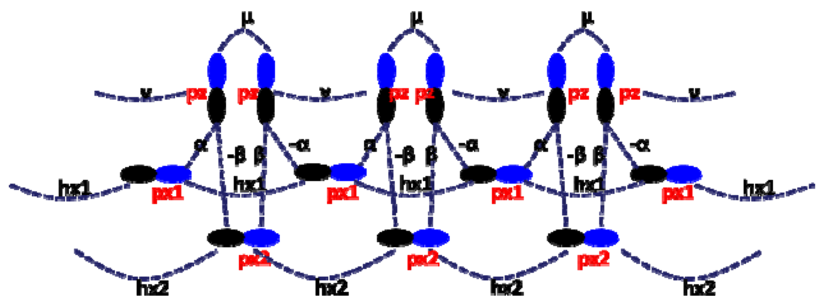


DB-derived bands in gap are used to build "DB logic gates"

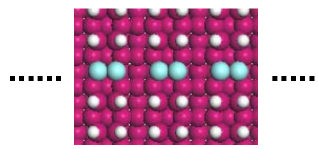
DB Switch: T(E) and I-V curves



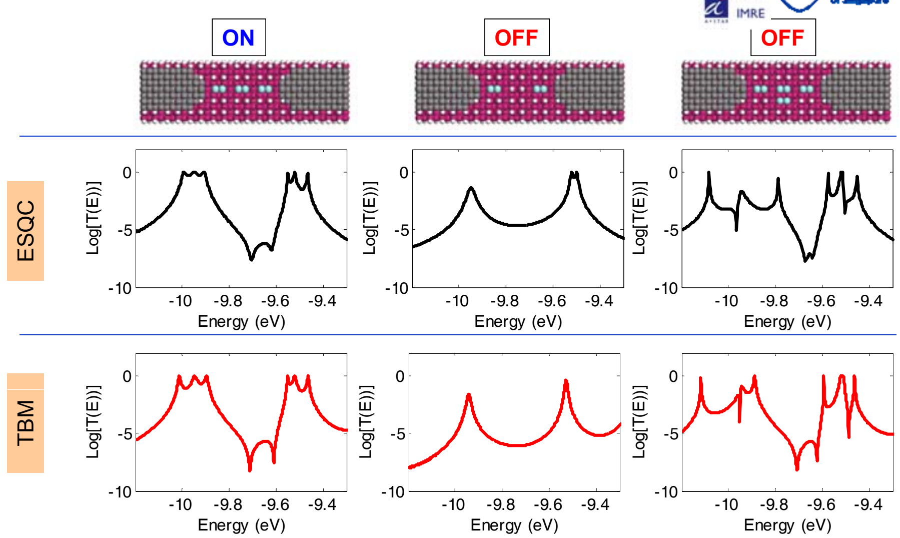
Tight-binding model for DB switch



Transport results from through-space and (more important) through-lattice coupling between DB pairs

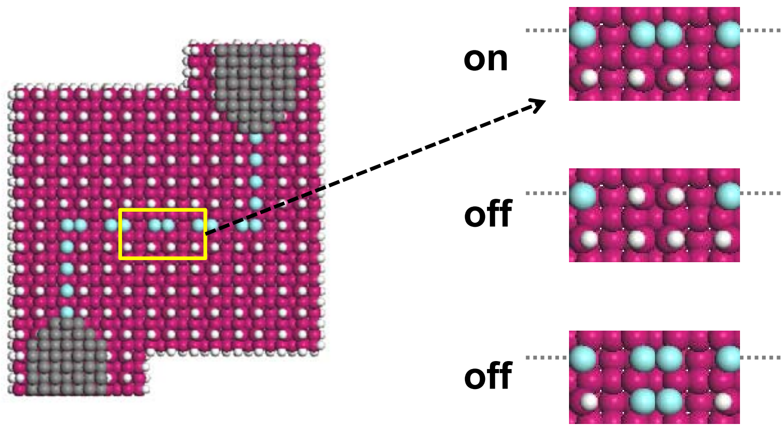


Tight-binding model for DB switch



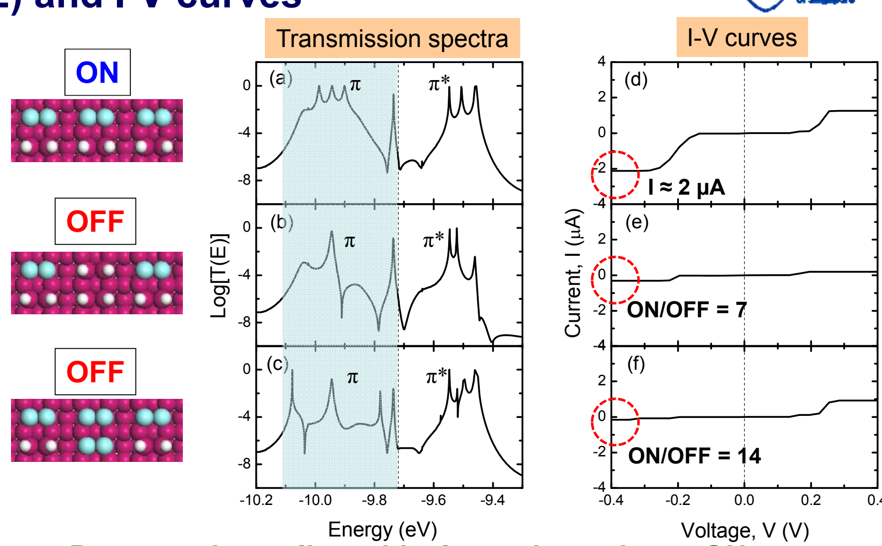
Qualitative agreement between TB model and full model.
TB model can be used to design large architectures.

Switch contacted by parallel DB wires



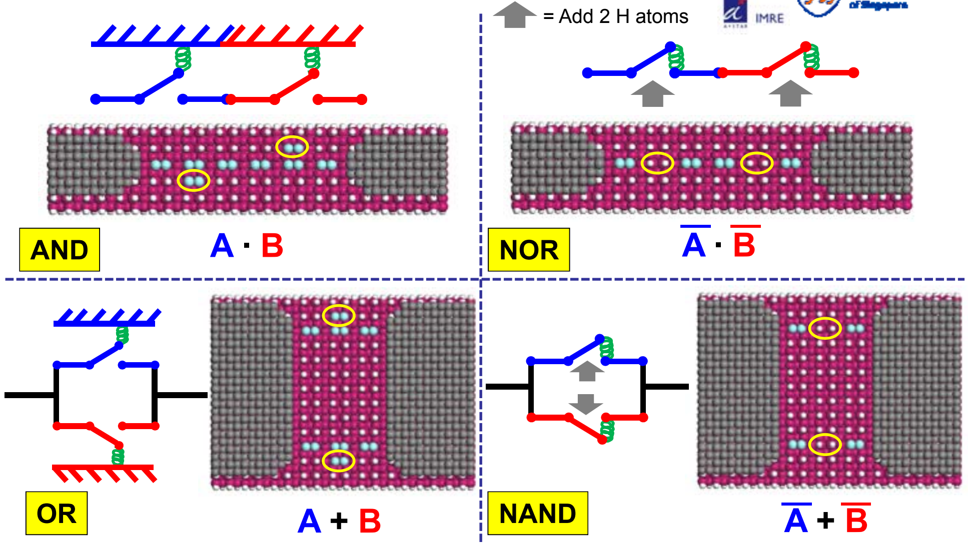
The switch can be contacted by parallel DB wires and keep its function. This provides flexibility to position the electrodes

Switch contacted by parallel DB wires: T(E) and I-V curves



Decreased coupling with electrodes reduces ON current, and consequently the ON/OFF ratio.

DB Logic gates: Parallel and Series



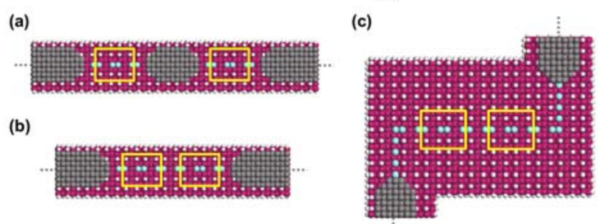
All 4 logic gates can be created by combining two switches in series or in parallel

Kawai et al., J. Phys.; Condens. Matter, submitted

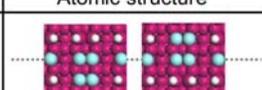
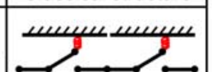
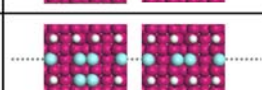
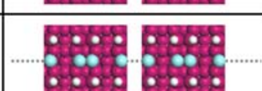
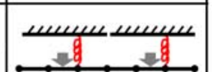
DB Logic AND gate on Si(100)-H

Switches connected in series

a) Through Au nano-wire
b) Directly
c) Directly, and connected by parallel DB wires

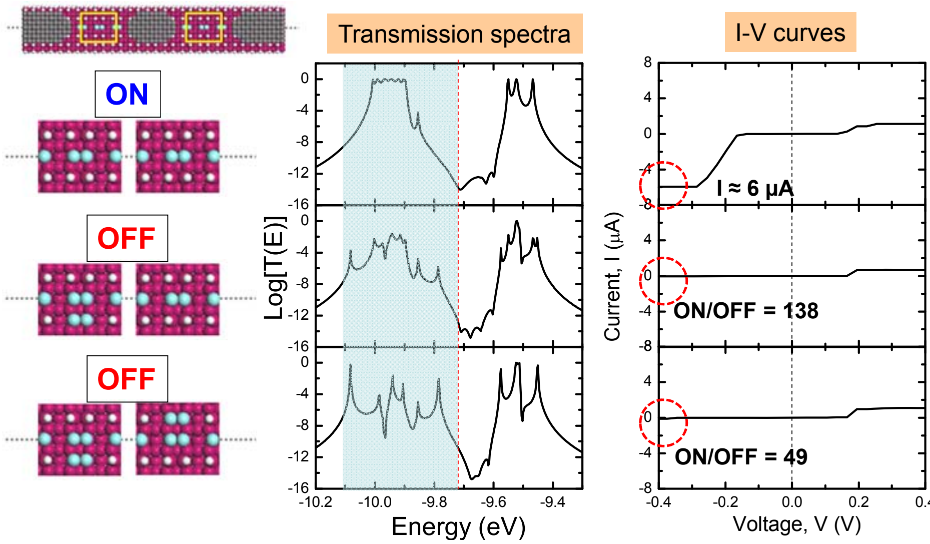


(d)

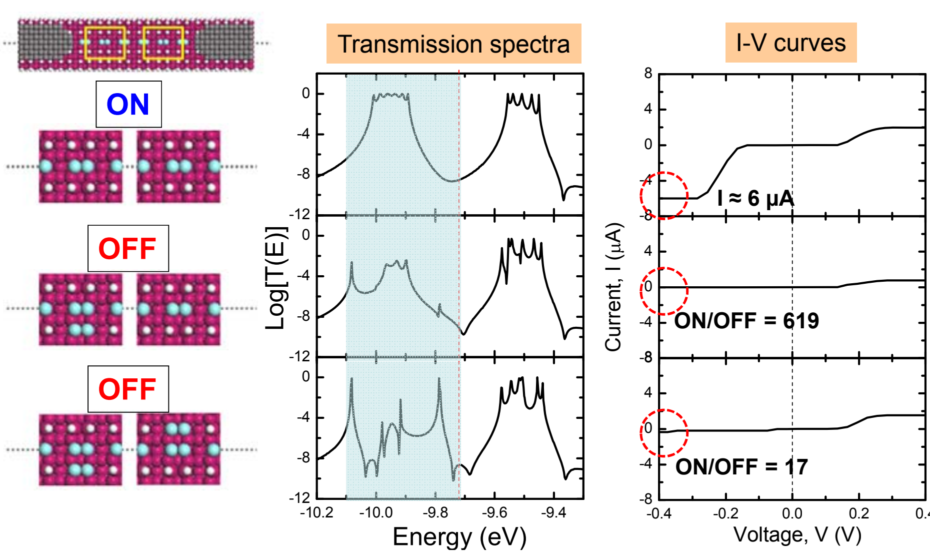
IN	OUT	Atomic structure	Classical structure
0 0	OFF		
0 1 1 0	OFF		
1 1	ON		

= Add 2 H atoms

DB Logic AND gate: T(E) and I-V curves



DB Logic AND gate without central wire: T(E) and I-V curves



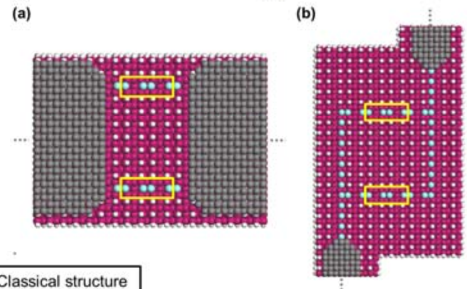
DB Logic NAND gate on Si(100)-H

AtMol IMRE NUS National University of Singapore

Switches connected in parallel

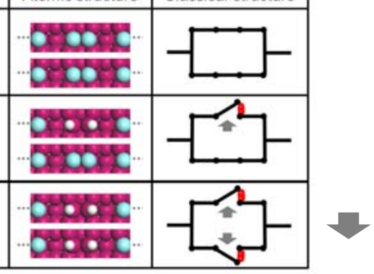
a) By a "large" Au pad

b) By parallel DB wires



(c)

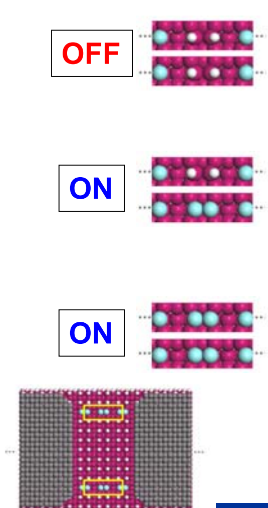
IN	OUT	Atomic structure	Classical structure
0 0	ON		
0 1 1 0	ON		
1 1	OFF		

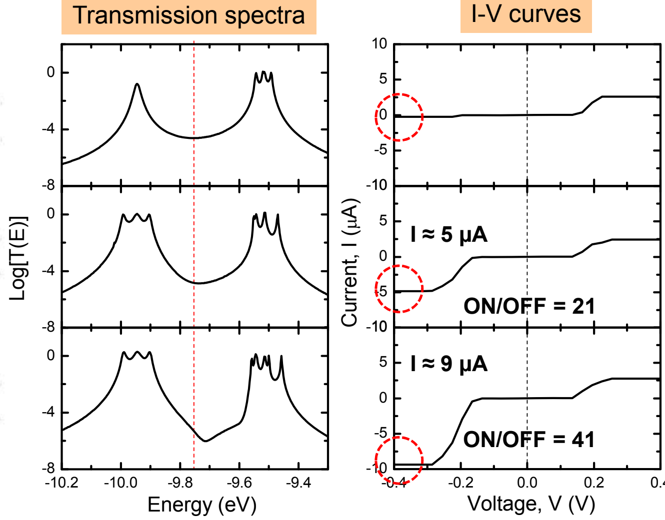


= Add 2 H atoms

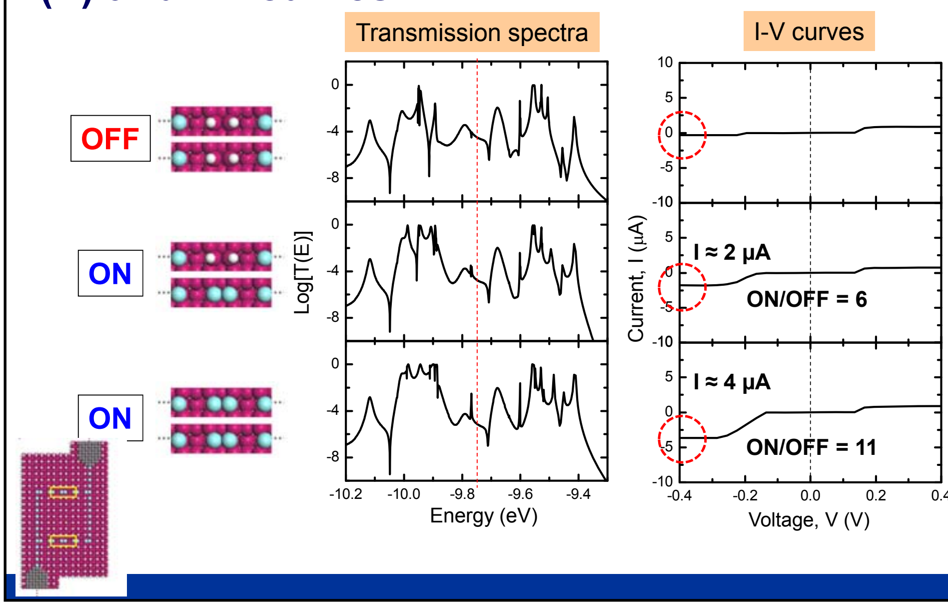
Kawai et al., J. Phys.; Condens. Matter, submitted

DB Logic NAND gate: T(E) and I-V curves

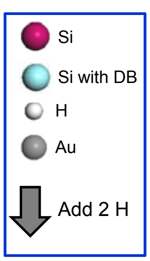


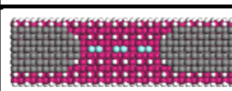
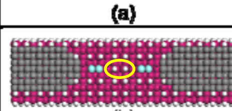
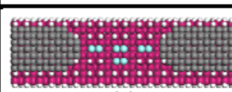
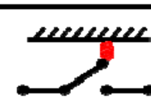
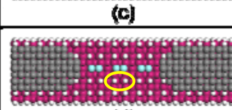
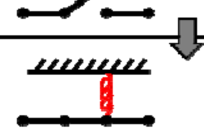


DB Logic NAND gate connected by DB wires: T(E) and I-V curves



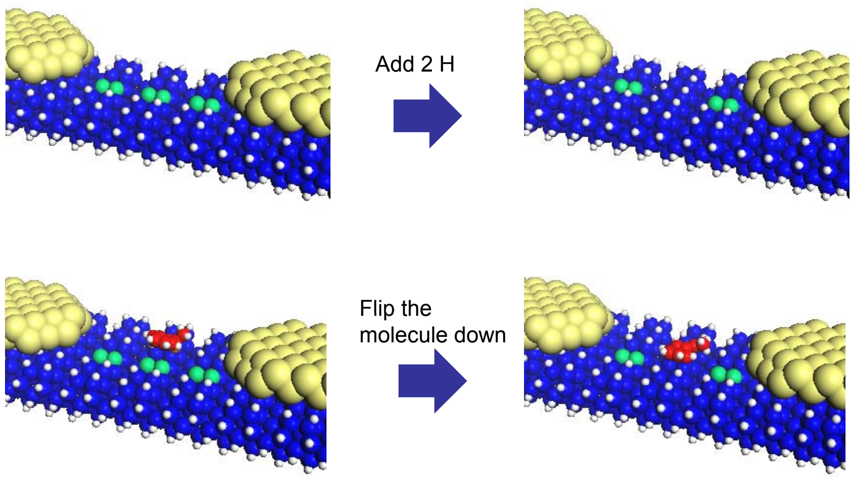
Switches on a Si(100) surface



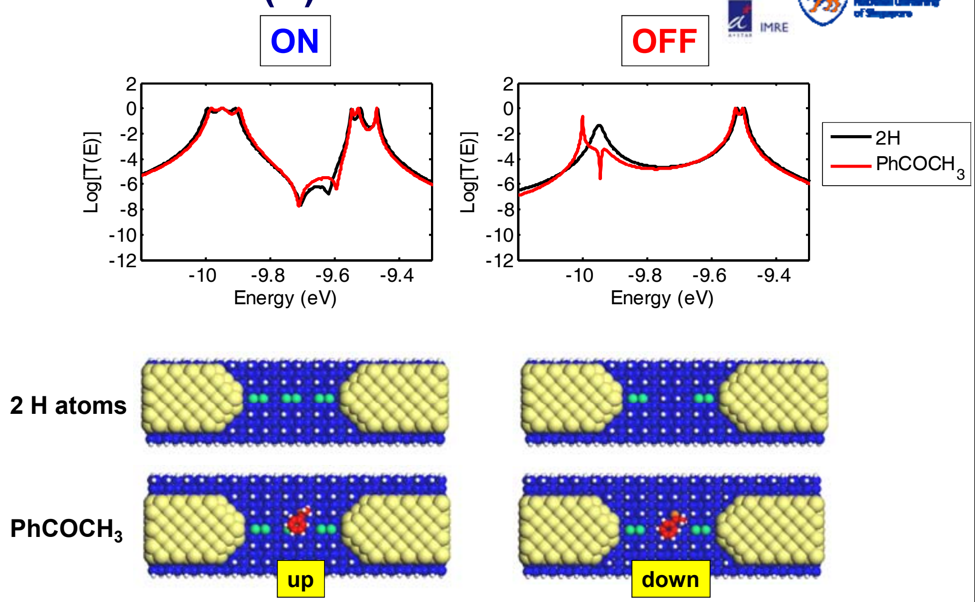
	IN	OUT	Atomic structure	Classical structure
Inverter	0	ON	 (a)	
Inverter	1	OFF	 (b)	
Follower	0	OFF	 (c)	
Follower	1	ON	 (d)	

How about more "practical" implementations?

Using a “switching” molecule



DB Switch: T(E) curves



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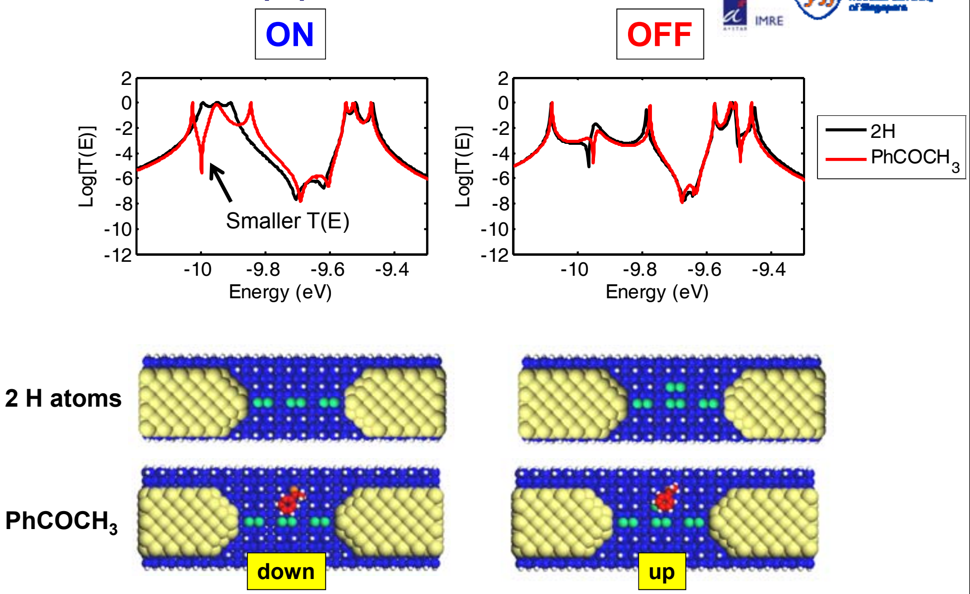
DB Switch: T(E) curves



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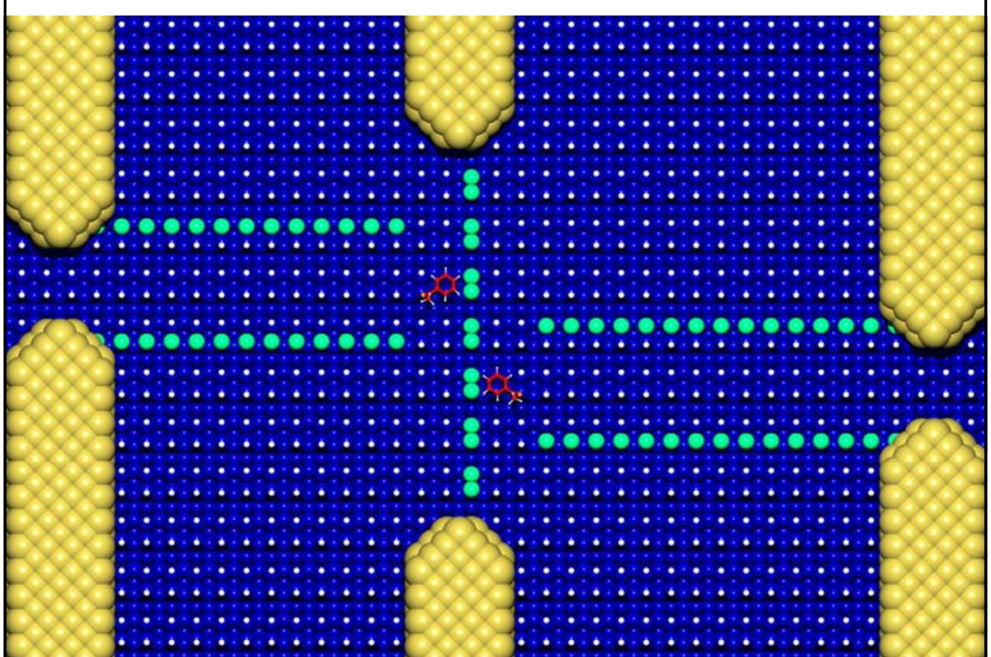

Conclusions

Dangling Bonds created on a Si(100)-H surface introduce states in the surface band gap

Two types of atomic scale switches were constructed using these DB states, and connected by DB wires

Four Boolean Dangling Bond Logic gates (2 input/1 output) were designed on a Si(100)-H surface, with ON/OFF ratio up to 100

Acknowledgements
A*STAR VIP at the Institute of Materials Research and Engineering
AtMol, Atomic Scale and Single Molecule Logic Gate Technologies
National University of Singapore