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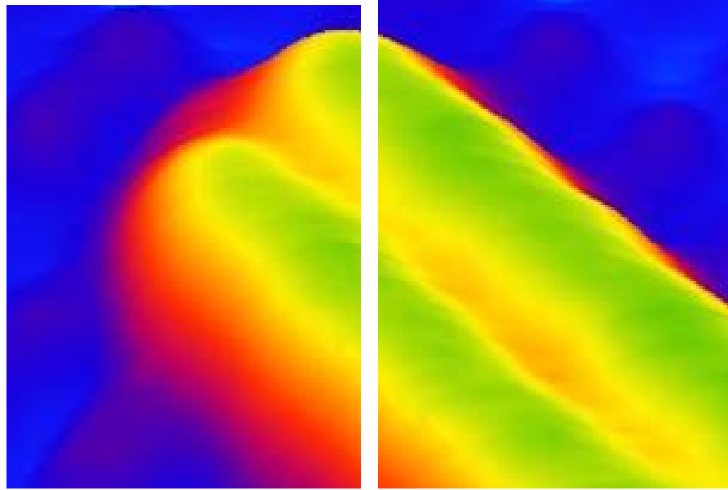
Atomic Scale and Single Molecule Logic Gate Technologies

AtMol



Atom by atom constructed dimer dangling bond wire on an Si(100)H surface

AtMol project

AtMol, ICT/FET Integrated Project (IP) funded by the European Commission, will establish comprehensive process flow for fabricating a molecular chip, i.e. a molecular processing unit comprising a single molecule connected to external mesoscopic electrodes with atomic scale precision and preserving the integrity of the gates down to the atomic level after the encapsulation.

AtMol

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Short facts

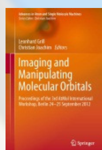
- AtMol — Atomic Scale and single Molecule Logic gate Technologies
- EC contribution — 6,9 M euros
- Contract number — 270028
- Nº of partners — 11
- Coordinator — CEMES-CNRS (France) / Christian Joachim
- Start date — January 01, 2011
- Duration — 48 months

2013 Publications Highlights

- M. Kolmer, A. A. A. Zebari, J. S. Prauzner-Bechcicki, W. Piskorz, F. Zasada, S. Godlewski, B. Such, Z. Sojka, and M. Szymonski "Polymerization of Polyanthrylene on a Titanium Dioxide (011)-(2 _ 1) Surface" Angew. Chem., 125, 1 (2013).
- C. Rauer, F. Rieutord, J. M. Hartmann, A. M. Charvet, F. Fournel, D. Mariolle, C. Morales and H. Moriceau "Hydrophobic direct bonding of silicon reconstructed surfaces" Microsystem Technologies, 19, 675 (2013).
- S. Godlewski, M. Kolmer, H. Kawai, B. Such, R. Zuzak, M. Saeys, P. de Mendoza, A. M. Echavarren, C. Joachim and M. Szymonski "Contacting a Conjugated Molecule with a Surface Dangling Bond Dimer on a Hydrogenated Ge(001) Surface Allows Imaging of the Hidden Ground Electronic State" ACSnano VOL.7 NO. 11 10105–10111 (2013).
- M. Kepenekian, R. Robles, C. Joachim and N. Lorente "Surface-State Engineering for Interconnects on H Passivated Si(100)" NanoLett., 13, 1192–1195 (2013).
- S. P. Jarvis, L. Kantorovich and P. Moriarty "Structural development and energy dissipation in simulated silicon apices" Beilstein J. Nanotechnol., 4, 941–948 (2013).

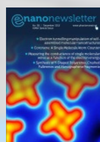
Further reading: www.atmol.eu/publi

Highlights



Imaging and Manipulating Molecular Orbitals

Proceedings of the 3rd AtMol European Workshop (Berlin)



E-nano Newsletter 28 (2013)

AtMol Special Issue

200 mm wafer where each chip has its back nano-interconnects and top encapsulation cap to access and protect atomic scale circuits by wafer bonding.