E-NANO NEWSLETTER

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REPORT: RANS

Status of Research into Architectures for Nanoelectronic Systems

15th NID

Press Release and Working Groups

GDR-E

GDR on Science and Applications of Nanotubes (NanoE)

PHANTOMS FOUNDATION

E-NANO NEWSLETTER

Dear Readers,

Welcome to the first issue of the "E-NANO Newsletter" that will three-monthly provide scientific articles, reports and updated information on Nanotechnology and more specifically Emerging Nanoelectronics.

Networking is vital to any scientist and even more so for persons working in the inter-disciplinary field of Nanotechnology. To fulfill this necessity, the “E-NANO Newsletter”, edited by the PHANTOMS Foundation (non-profit organisation based in Madrid, Spain) will provide comprehensive and updated information on latest advances in Emerging Nanotechnologies. In this way, this initiative achieves the aim of both raising the awareness of scientists in Nanotechnology and aiding them in developing beneficial collaborations and employment opportunities.

This newsletter will also publish relevant information about Integrated Projects funded by the European Commission such as NaPa (Emerging Nanopatterning Methods - NMP) aiming at developing new technologies such as nanoimprint or soft lithography and Pico-Inside (IST/FET/NID) that will explore Atomic Scale Technology with the final goal of integrating a complex logic gate inside a single molecule.

A selected range of emerging R&D activities such as Molecular Electronics is expected to strategically impact on future developments in the nanoelectronics domain and their long-term applications. Crucial issues such as modelling the behaviour of these possible nanodevices and the definition of system architectures need to be addressed.

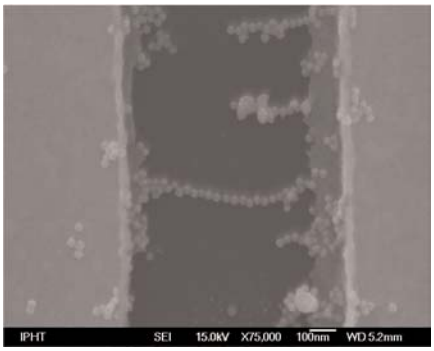
In this first issue, we therefore publish a report prepared by Prof. Mike Forshaw (University College London, UK) on the “Status of Research into Architectures for Nanoelectronic Systems in the European Research Area” and the conclusions of the Working Groups (Molecular Electronics and NEMS) held during the NID15 Workshop in Madrid (February 2005).

These working groups (http://www.phantomsnet.net/Enano/WorkingGroups.php) are open and we invite readers to contact coordinators to provide inputs & comments to improve these initiatives. The next NID16 event will take place in Glasgow (UK): June 22-24, 2005 - http://www.phantomsnet.net/nidconference10.php

We also invite readers to send us their scientific contributions either as articles, reviews or publication highlights.

We would like to thanks all the authors who contributed to this issue as well as the European Commission (IST/FET/NID) for its close collaboration.

Dr. Antonio Correia
PHANTOMS Foundation
Editor



Cover Picture: *The image shows a one micrometer gap (gold electrodes, 100 nm thick) on silicon oxide, with a single file of gold nanoparticles (30 nm diameter) captured using dielectrophoresis.*
R. Kretschmer and W. Fritzsche: Pearl Chain Formation Of Nanoparticles In Microelectrode Gaps By Dielectrophoresis. Langmuir 20(2004), 11797-11801
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The Status of Research into Architectures for Nanoelectronic Systems in the European Research Area (RANS).

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Introduction

This short report is the outcome of a one-month study, funded in late 2003 by the European Commission (IST / FET), into the status of research into architectures for nanoelectronic systems. Here we use the term 'nanoelectronic system' to mean any assembly of data processing devices (electronic, magnetic, superconducting etc.) where one or more of the characteristic device dimensions is of the order of 100 nanometres or less. The reason for the study is that, although there are many nanodevices currently under investigation, there is relatively little research into how some of these devices might behave if they were to be assembled into circuits or large systems. The emphasis in this report is on large-scale digital systems. A more comprehensive EC-funded follow-on study was carried out in 2004, which also considered nanophotonic, analogue, mixed analogue-digital and other systems. The report for this later study (Nano Arch 04) is available from the first author (m.forshaw@ucl.ac.uk).

It is hoped that this report will act as a stimulus to guide subsequent activities in the field. Its original terms of reference were to provide an outline of:

1. Existing and proposed devices
2. Small and ultra-large circuits: theory and practice
3. Conventional architectural concepts, 'System on a chip', 3D systems et cetera.
4. Known problems
5. Unconventional and new concepts
6. Applications – performance requirements
7. Availability and training of human resources

These are considered in the sections which follow, but we first discuss what we mean by "architectures for nanoelectronic systems". It has been suggested that there are five levels which must be looked at before the performance of an electronic system can properly be assessed (e.g. Meindl 01). These are:

the fundamental level (quantum effects, thermodynamic effects etc.),
the materials level (silicon, GaAs, molecular, polymer etc.),
the device level (field effect transistor, rapid single flux quantum, quantum interference, etc),
the circuit level (analogue versus digital, A-to-D converter, 64-bit full adder, memory array etc.) and
the system level (e.g. achieving Teraflops processing speed at less than 1 megawatt power dissipation).

To this one might add a sixth level, namely the application or cost level: if a device technology is not sufficiently promising for some proposed application (because it will not be faster than CMOS, or cheaper, or more reliable, or...) then it would be helpful to know this as soon as possible. Research is needed at all of these levels, although not necessarily simultaneously or with the same level of effort. Figure 1 shows that although 'nanoarchitecture' is a relatively high-level concept, it has links all the way down to individual devices and to the device technology.
In many cases research at higher levels can only be made in very general terms, because the properties of some devices are not known sufficiently well. On the other hand some device technologies have reached a state of development where circuits with thousands or even millions of devices have been fabricated, sometimes at a near-commercial level. However, it is usually true that these large-scale circuits use devices whose technologies

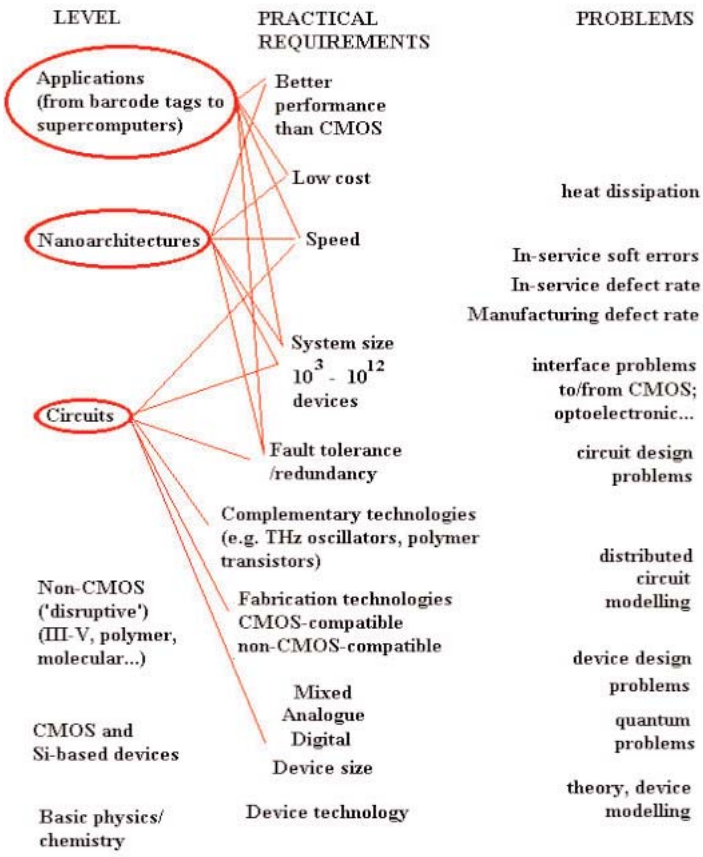

Figure 1. A simplified table to show the relationship between architectures for nanoelectronic systems and other hierarchical levels, together with some of the technical requirements and the problems that have to be solved at each level

are relatively mature, and where the problems associated with the nanoscale (quantum effects, noise, fabrication problems etc.) are manageable. If these last devices were to be miniaturised, in the same way that silicon-based CMOS transistors have been miniaturised for the last thirty years, then they too would start to encounter many problems, which sometimes have no known solution.

Of course, there are many factors which have to be considered. Many of these devices - for example molecular devices - are at an early stage in their development, and there may not be enough information available to predict their performance, if they were to be combined into large structures. On the other hand, some devices - for example single-walled carbon nanotube transistors - have already been assembled into small circuits, and it is clearly necessary to start thinking about their possible performance in very large circuits. There are devices, such as polymer transistors and photonic structures, whose current dimensions are tens of micrometres, but which could well be made much smaller, or used to interface with nanoelectronic circuitry. One should also mention the major problems associated with quantum phenomena, which allow nanodevices to work, but will cause serious problems when many such devices are combined in closely-coupled circuits.

For other reviews of architectures for nanoelectronics the reader is referred to Stan 03, Waser 03 and Forshaw 04. The last paper

was partly funded as part of the present study. The updated version of the 2003 International Technology Roadmap for Semiconductors has a chapter on research devices, which contains a short section on architectures (ITRS 04).

1. Existing and proposed devices

It is not the purpose of this study to review existing or proposed nanodevices in any detail, only to illustrate their spread in development status, from the device to the system level. Figure 2, which is updated from [Nikolic 03], shows that there is a spectrum of development status, from individual experimental devices to fully commercial systems that contain nanoscale features. If we suppose that the last three columns in Figure 2 ("subsystem" to "big chip") represent the domain of "nanoarchitectures", then it is clear that most devices are as yet architecturally undeveloped.

It is the opinion of some workers that many of these devices will not proceed beyond the research stage, and that those that do proceed to commercial production will be *complementary* to CMOS, rather than *replacements* for CMOS.

Device Name	Single Device	Simple Circuits	Logic Gate Mem. Cell	Sub-system	Small Chip	Big Chip	Comments
CMOS							Approaching the scaling limit
Magnetic random access memory (MRAM)							Non-volatile; no complex circuits
Rapid single flux quanta (RSFQ)							Extremely fast but needs cooling
Organic transistors							Cheap, large, slow, may shrink further
Resonant-tunnelling diode-HFET (III-V)							Fast, but high power
Single electron transistor (SET) memory							Small, but not yet reliable
Bulk molecular logic/memory							Potentially down-scalable
Nanotube/nanowire transistors							New devices reported regularly
Quantum cellular automata/magnetic (MQCA)							Room temp.; limited results so far
Resonant tunnelling diodes (RTDs) (Si-Ge)							Potentially useful but hard to make
Magnetic spin-valve transistors							May be miniaturizable
Quantum cellular automata/electronic (EQCAs)							Low power, but very hard to make
Josephson junction persistent current qubit/cubit							Could be used in a quantum computer
Single electron transistor (SET) logic							Circuit design/fabrication is hard
Molecular (hybrid electromechanical)							First single-molecule transistor
Quantum interference/ballistic electron devices							Problems with lack of gain
Mono-molecular transistors and wires							The smallest devices possible

Pre-fabrication phase: no information; theory; simulation

Fabrication phase: agony/struggle; working demonstration; commercial or available

Figure 2. Development status of various nanodevices and devices with nanoscale features. The headings 'single device….big chip' are intended to indicate in qualitative terms the relative scale of progress towards making chips with more than 108-109 devices on a chip. No attempt has been made to distinguish between devices that are suitable for logic or memory applications. Updated from [Nikolic 03].

2. Small and ultra-large circuits: theory and practice

Because of the variations in their level of development, some devices have been built at the large scale, for example magnetic random access memory (MRAM) and rapid single flux quanta (RSFQ) chips; some at the small scale, for example small logic circuits with semiconductor nanowires or carbon nanotubes; and some devices have not yet been built - for example single-molecule logic circuits. The main drive for nanoelectronic circuits seems to be aimed at developing systems that have more processing power per unit volume than (future) silicon-based circuitry. This would imply device densities of the order of more than 10^{10} cm^{-2} for logic-based circuitry and more than 10^{11} cm^{-2} for memory devices. However, it is clear that, as devices get smaller and smaller, so their maximum operating speed at high device densities, which is linked to the device power dissipation, may be often be *less* than that of present-day CMOS (see section 6 for a brief discussion and example). This implies that there may be:

either a limit to the number of devices on a chip (this section),
or that parallelism will be needed (see section 3),
or that devices with improved specifications will be needed (section 3),
or that new concepts will be needed (section 5).

Not all applications require circuits with huge numbers of devices. For example, commercial applications of polymer-based transistor circuits currently require less than a few hundred devices, while many automotive or white-goods applications only need microprocessors with less than a million devices. Admittedly, these do not require nanoscale devices, but there are applications (for example, medical) where relatively small numbers of devices (less than 10^6) are needed, but in as small a volume as possible. However, the main thrust of development in Si-based systems lies on the axis: palmtop - laptop - desktop - supercomputer, where the maximum possible number of devices is wanted, and it is probable that most nanoscale systems will be compared with, and assessed against, the nearest Si-CMOS benchmark.

Any new or proposed nanoscale circuits or systems must first be assessed against a Si-CMOS benchmark. Some applications may need only small systems, some extremely large, but no nanoscale system will be successful unless it outperforms the Si benchmark in some way (cost, speed, size, etc.).

3. Conventional architectural concepts, 'System on a chip', 3D systems

The term 'computer architecture' is a concept which, to some degree, is *independent* of the hardware that is used. Thus digital computers have been made using mechanical gears, electrical relays, thermionic tubes, individual transistors, integrated circuits, rapid single flux quanta devices, optoelectronic hardware, DNA-related molecules, and so on. 'Analogue' (or probabilistic-output) computers have been made using operational amplifiers, sub-threshold CMOS circuits, special-purpose digital circuitry, and simulation programs running on conventional computers; while Nature has had several billion years of development time to produce a wide range of biological data-processing structures.

In principle the term 'computer architecture' should be divorced from its practical implementations, because it is often considered to be a high-level theoretical construct. In practice the term has a significantly different meaning to different people, depending on the individual's technical background and experience. In this report we therefore take a more broad-brush approach, and allow the term to include areas such as the high-level influence of practical applications on computer design, all the way down to circuit design and individual device characteristics at the low level. Equally, we shall blur the distinction between theoretical concept and practical implementation, since it is often the case that physical and technological constraints and performance demands will affect the physical structure of a computer, while device properties may affect the layout of small-scale circuits and the classes of problems that the computer will be most efficient at solving.

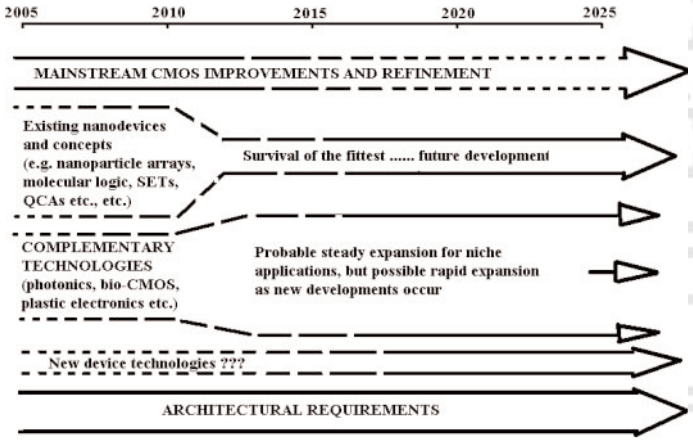

Figure 3. Possible timelines for future nanoelectronics development. Architectural factors as described in the text will apply to all of the timelines. The relative width of the bars has no special significance.
(from Nano_Arch 04)

Such interactions at all levels between device characteristics, application requirements and technological constraints, and architecture (Figure 3), will be as important for post-CMOS systems as they are for present-day CMOS systems.

People have been investigating and developing computer architectures for sixty years, trying to increase their performance. There have been tens of thousands of publications in this area, and it is not the purpose of this report to review the field in detail. As far as architectures for nanoelectronic systems are concerned, the most relevant concepts are:

Parallelism - the use of more than one processing element, often identical and arranged in a relatively simple geometry such as a rectangular mesh or perhaps a more complicated geometry such as a hypercube or a fat tree. Parallelism *sometimes* offers massive speed increases over a single, general-purpose processor. Modern PCs or workstations, although they use limited forms of parallelism, are lineal descendants of the original, von Neumann, single-processor concept. Parallelism also offers the possibility of using huge numbers of relatively small, slow, processing elements to outperform fast, powerful, single processors. However, the single-processor concept has the advantage of flexibility – it can in principle be programmed to solve any problem – whereas highly parallel systems are sometimes very inefficient, except when they are designed to solve specific classes of problem.

Specificity - tailoring of the hardware to match the requirements of a particular algorithm - for example, the Fast Fourier Transform, or image processing tasks - and thereby to achieve the maximum possible speed. The disadvantage of this speedup is that the hardware is no longer 'general purpose' – the only calculation that it can carry out efficiently is the chosen algorithm. This limitation can partly be avoided by using reconfiguration techniques.

Reconfiguration - the ability to 'rewire' a generic arrangement of simple elements (memory or logic) to implement some desired function. Existing memory chips have a simple form of reconfiguration - spare rows or columns of memory cells can be switched to replace cells that are found to be defective during manufacturing. A more sophisticated form of reconfigurability is available through the use of (Field) Programmable Gate Logic Arrays (FPGLA). In the context of nanoelectronic systems, perhaps the most famous example of a reconfigurable computer system was the Teramac, which also demonstrated an implementation of fault tolerance.

Fault tolerance - the ability of a computer system to operate reliably, even if many of its individual components suffer from manufacturing defects, from in-service failures, or from random transient errors. Fault tolerance requires the use of an architecture which can implement whichever fault tolerance algorithm has been chosen. The term 'fault tolerance' is sometimes invoked as a mantra, in the belief that useful, high-performance, nanoelectronic systems can eventually be developed, no matter how defective or faulty the individual nanoscale components might be. This belief should be treated with considerable scepticism: in some cases, fault tolerance may require such large numbers of spare components that the resulting system may be *less* efficient than a system that uses larger but more reliable components.

System on a chip - the integration of different technologies on a single chip. These could be different digital technologies (CMOS, Si-Ge, III-V), or mixed analogue (photosensors, chemical or biosensors) and digital; optoelectronic; mechanical (NEMS/MEMS); hybrid systems (CMOS/molecular); etc.

Asynchronous operation - it has long been known that digital systems do not need to have a master clock, but it is only recently, with increasing power and space demands involved in generating chip-wide clock signals, that systems which use local clocks and data handshaking, have started to look attractive.

Short range data/control signals - this concept overlaps that of asynchronous operation. Instead of having a master controller to distribute control signals over the whole of a chip, it is possible in some circumstances to have only a limited number of master control lines, and to rearrange the system layout so that individual processing elements in a large array operate semi-independently from one another. This concept is related to the MIMD – SIMD classification of computer types. MIMD stands for Multiple Instruction, Multiple Data: a network of PCs in an office is an example of an MIMD system. SIMD stands for Single Instruction, Multiple Data – the 'retina-like' CLIP (cellular logic image processing) arrays of the 70's and 80's, and the more recent CNN (cellular neural network) systems, are examples of SIMD systems. 'Neuromorphic' systems can be considered to be extensions of CLIP or CNN concepts, which in turn overlap with fault tolerant cellular automata structures (e.g. [Peper 03]).

Finally we may mention **3D systems**. The main advantage of '3D' systems is that one can pack more devices into a given footprint: the main disadvantages are that it is relatively hard to send signals throughout the volume, and heat dissipation problems rapidly increase in severity. The simplest way to make a 3D system is to stack 'ordinary' chips on top of each other: this has been done with conventional Si-based chips for many years, and in a variety of ways. Two chips can be relatively easily connected 'face-to-face' using 'flip-chip' techniques, but until recently stacks of three or more chips have mainly been connected 'edge-to-edge'. A recent EC-funded project examined ways to provide through-chip vias and 'face-to-face' molecular wiring between chips [Crawley 03]: a book on this subject was published in October 2004 [Crawley 04]. There has been a recent US DARPA call for proposals to develop 3D stacks of (Si-CMOS-based) chips.

There is a large body of existing literature on architectural concepts, but new techniques continue to appear. The application of both old and new ideas to nanoelectronic systems has only just started.

4. Known problems

More and more problems have to be overcome as device sizes approach the nanoscale. The most dramatic evidence for this, at least for Si-CMOS devices, is presented in the ITRS Roadmap tables, where unsolved problems are shown as 'red brick walls' [ITRS 04]. The same will be true for any other nanodevice, nanocircuit, nanoarchitecture or nanosystem. In general terms, the problems are quite well understood: they range from quantum effects to reliability problems, as shown schematically in Figure 1 in the Introduction. It is (sometimes) relatively easy to analyse one problem in isolation. For example, a single-electron transistor at zero Kelvin, with 'perfect' contacts and power supply, can be analysed to a fair degree of accuracy; or the quantum mechanical probability of electron transmission near equilibrium through a small molecule at zero Kelvin, again with 'perfect' contacts. However, it is much harder to include finite temperature effects, non-equilibrium electron transport and the existence of many similar devices in close physical contact. Yet again, at the other end of the scale, fault tolerance techniques have been developed over many years, but the effects of defects or transient errors on the performance of large nanosystems have yet to be examined.

It is not the aim of this report to provide an exhaustive analysis of these problems. Here we present instead two simple examples to show that there are many problem areas where much further work is needed before the properties of nanocircuits and nanosystems can be predicted with any degree of certainty.

The first example is illustrated in Figure 4, which shows a hypothetical six-transistor memory cell with six single-electron transistors (SETs). The small circles represent the islands of the SETs. In a 6T memory cell using conventional Si transistors, a first-order analysis of the circuit behaviour is (relatively) straightforward, because the inputs and outputs are more or less isolated from each other. However, Figure 4 shows that the SET layout will behave as a *distributed* capacitative network, whose analysis is complicated even further by the quantum blockage effects involved in the SET operation. This picture (of an unworkable circuit!) is intended only to illustrate how electrical coupling between neighbouring conductors and distributed capacitances may start to dominate circuit operation as devices and wiring become smaller and smaller. In general the electrical isolation between the input and output of any device becomes worse as the device shrinks in size. Circuit design techniques to analyse distributed capacitative or electromagnetic coupling effects at a classical level are relatively well developed, and the theory of SET operation in, for example electron pump circuits, is quite well understood, but nobody has yet tried to analyse the combination of multiple–SET circuit behaviour with distributed capacitative effects.

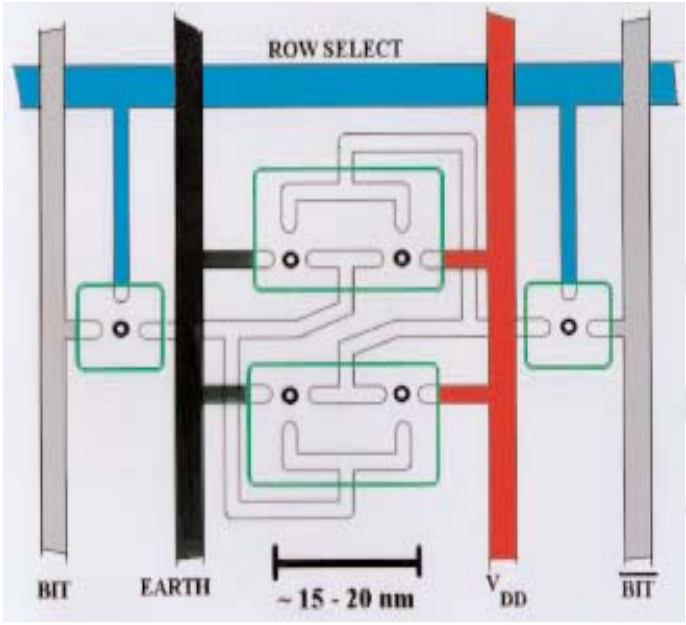

Figure 4. A hypothetical single-electron transistor 6T memory cell.

Our second example is taken from the field of fault tolerance and error correction. The problem of error correction for nanodevices and nanocircuits is not an academic one, whose possible consequences can be ignored for ever. Even present-day CMOS chips, with minimum feature sizes in the 130 – 90 nm range, now have to take account of soft errors due to radioactive decay products and cosmic rays. Much 64-bit on-chip memory now has error coding and correction (ECC) built in to overcome soft errors, and as devices get smaller so soft error rates (SER) will go up. To quote from a recent paper (Baumann02).

"SER has become a huge concern in advanced CMOS products because, uncorrected, it induces a failure rate higher than all the other reliability mechanism combined".

So far CMOS logic devices, which typically use larger-than-minimum features than memory, have not been of such concern, but SER in CMOS logic is also becoming a problem. The use of triple

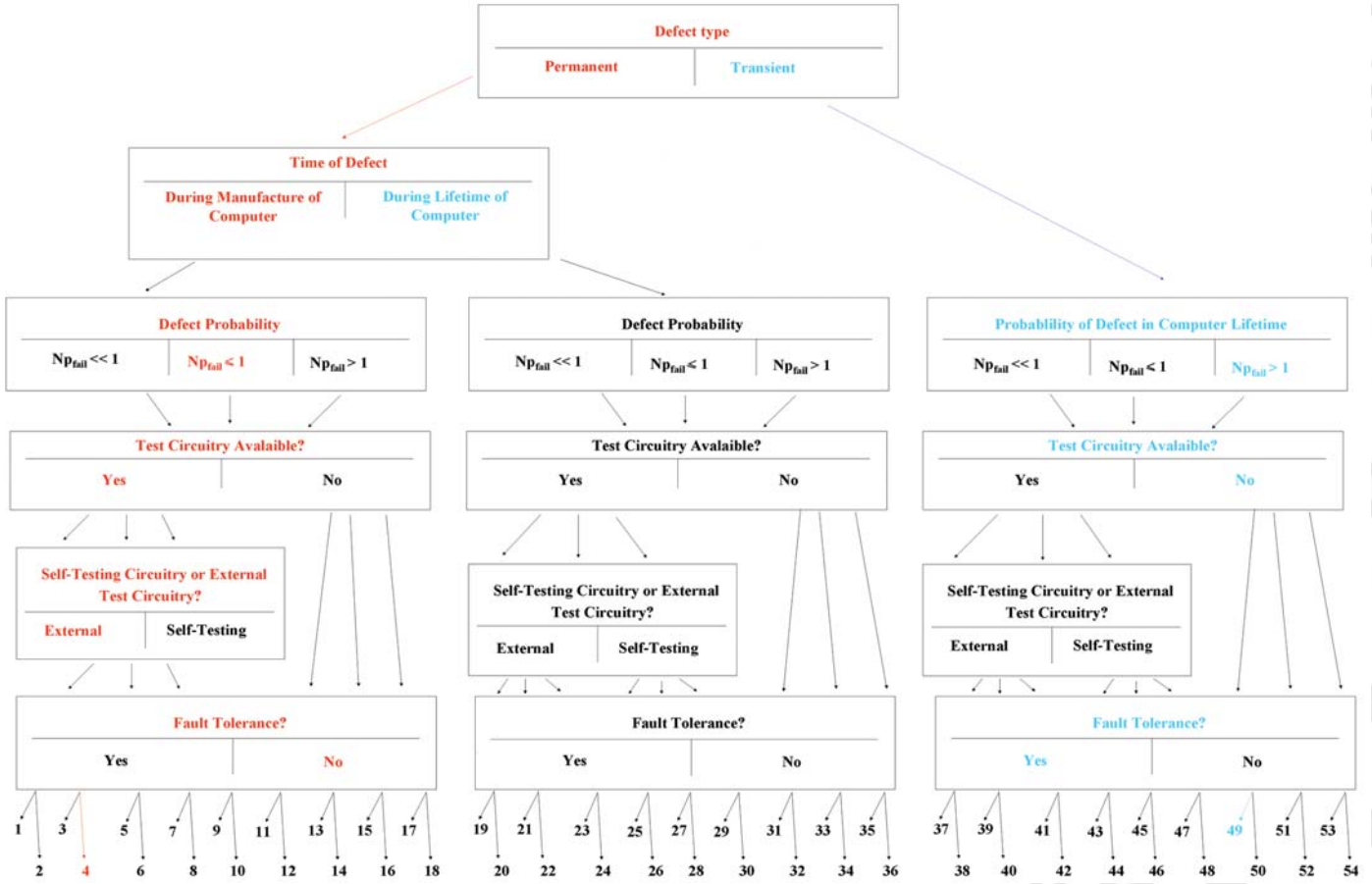

Figure 5. A simplified flow chart to illustrate the variety of strategies that can be adopted, given the possibility of permanent defects or transient errors in a (nano) electronic system. The left path is representative of the present-day strategy for producing reliable memory chips (using spare rows or columns of memory cells). An example of the strategy involved in the right path is the use of Triple Modular Redundancy (TMR), which is used in passenger aircraft flight control computers.

modular redundancy (TMR), with three copies of the logic circuitry, is being talked about, even for one-chip single-user commercial operation [Baumann 02].

If fault tolerance and error correction are needed for present-day CMOS chips, where transistors have minimum feature sizes of 130 - 90 nm, then it is clear that future nanoelectronic systems will have an even greater need for careful design to protect against hard and soft errors. Once again, relatively little work has been carried out in this area. Figure 5 shows that a wide range of strategies are available, with some being more effective than others (*N* denotes the number of devices involved, p_f denotes the failure rate per device). It will certainly be necessary to combine more than one strategy if reliable nanosystems are to be produced. There are relatively few different techniques available for providing fault tolerance. Figure 6 illustrates the underlying problem. Suppose that one wanted to manufacture a chip with 10^{12} nanodevices, each having a manufacturing failure rate p_f . Three techniques are compared – R-fold Modular Redundancy (an extension of TMR), von Neumann's multiplexing technique, and system reconfiguration (cf. [Nikolic 01, 02]). Figure 6 shows that the best protection against manufacturing faults is reconfiguration. However, to produce chips with a 90% probability of working (for example), if the manufacturing defect rate for an individual device is 10%, a factor of at least 30-fold device redundancy is needed, and this factor does not include the extra redundancy needed to make the system reconfigurable in the first place. To achieve three-fold redundancy (again, for example), a device failure rate of less than ~10^{-5} will be needed. This is only slightly less challenging than the failure rate of present-day CMOS devices (which is, *very* approximately, in the range 10^{-6} to 10^{-7} per device). We note in passing that much has been talked about about the possibilities of self-assembly for making nanoscale circuits and systems, particularly for molecular devices. However, there have as yet been very few demonstrations of the controllability or reliability of self-assembly.

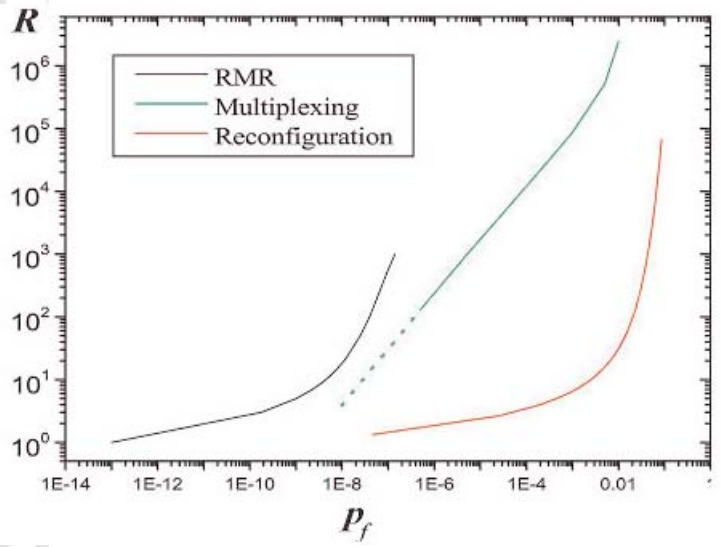

Figure 6. Comparison of three fault tolerance strategies in protecting a hypothetical chip with 1012 nanodevices against permanent manufacturing defects. R is the redundancy factor (the number of copies of each device or circuit), and pf is the failure rate per device. From [Nikolic 02]. See text for details. Recent work (2004, 2005) has shown that reconfiguration can provide dramatically improved results, i.e. moving the red curve rightwards and downwards

Analysis tools for individual nanodevices exist, but with varying degrees of analytical approximation. Tools for nanoscale circuits containing tens or hundreds of devices are as yet very primitive or nonexistent. At the system level, the effects of manufacturing defects or transient in-service errors will make very severe demands on the amount of circuit redundancy that will be needed for reliable operation: these constraints have yet to be analysed fully.

5. Unconventional and new concepts

In the field of nanoelectronic systems there is almost no such thing as a completely new concept: almost all "new" ideas have their origins in earlier concepts (Feynman's "There is always room at the bottom" perhaps being the exception). In this section we briefly discuss some unconventional ideas and 'new' concepts, but it should be appreciated that these sometimes have a previous history of development.

Although analogue computers largely gave way to digital computers, they have never completely disappeared, and they may offer some significant advantages at the nanoscale. Certainly, analogue-digital circuitry has undergone a significant expansion over the last few years. Some cellular neural network (CNN) chips have mixed analogue and digital circuitry, and the System-on-a-Chip concept is largely aimed at combining analogue sensors with digital processing. Combining analogue data processing with digital processing has also been shown (in principle) to offer advantages in terms of efficiency in speed and in heat dissipation [Sarpeshkar 98]. Many more 'exotic' concepts have been described – for chemical computers, DNA computers, microfluidic processors and so on. These will be considered in the briefly in the following sections.

Extensive research on animal brains has demonstrated their superlative efficiency in power consumption, in parallelism and in processing power [Laughlin 03], but so far there have been few attempts to make close copies of the complex bio-electrochemical processes involved. Some of the principles involved in neuronal processing have, however, been copied extensively, in all sorts of ways, from software neural networks running on conventional computers, to the use of subthreshold CMOS devices working like synthetic neurons, and on a variety of mesh-connected computers that emulate some aspects of the visual retina and/or higher-level cortical processes (e.g. CLIP, CNNs).

It was shown more than thirty years ago that the cellular automaton game 'Life' was a universal computer, and students at MIT modelled a logic gate using Life. However, it occupied about a million cells. Very regular arrays of very simple processing elements are usually very inefficient at solving real-world problems, although systems using two-dimensional arrays of nanoparticles continue to be described and analysed (e.g. [Csaba 01], [Basu 04]). The choice is to move away from perfectly regular meshes, while still using cells with very simple properties – the quantum cellular automata (QCA) approach – or to use regular meshes of cells with more processing power in each unit – the CNN approach. So far the QCA approach appears to be subject to a variety of serious problems, not only in implementation, but also in performance [Parish 03]. Similarly, as anyone who has designed, built or used a highly-parallel processing engine will know, cellular nonlinear (or neural) networks (CNNs) are intolerant to device failure, which is likely to be extremely important with future nanodevices. It is equally difficult to avoid problems with system clocking and data distribution, although several asynchronous array structures have been proposed as possible candidates for nanocomputers (e.g. [Peper 03, Peper 04]). Thus the trend in cellular logic, CNN, and cellular automata research has been towards building-in fault tolerance.

Some new ideas

Many interesting ideas have been put forward over the last few years. Some of them have been aimed at protecting nanoelectronic systems against manufacturing faults or against transient faults that might occur in-service. We present here some extremely brief descriptions of these different ideas.

It is generally accepted that nanoelectronic systems will probably have to have extremely regular structures (like cellular automata or CNNs), so that they can be made easily, perhaps using self-assembly techniques (see below). Because of the inherent attractiveness of the ideas behind field-programmable gate arrays (FPGAs), some concepts have combined the regularity of CNNs and FPGAs at the local scale with the assumption that larger-scale structures will look like reconfigurable systems.

Likharev has proposed a relatively complex architecture, which is based on regularly structured elements which are laid out in a crossbar geometry [Likharev 04]. The details are too complex to go into here, but the processing elements are essentially 'neurons' with a relatively standard sum-and-threshold behaviour. It is assumed that the processing devices will be single-electron transistors and single-electron traps which act as local memory. High performance levels in the presence of defective or noisy devices have been reported.

The NanoCell concept is illustrated in Figure 7. A 'large' region of insulated substrate is filled to a suitable density with a sparse layer of nanoparticles, then molecular wires are quasi-randomly deposited on top, so that some of them touch the nanoparticles and some of them touch a number of contact pads at the edge of the region. By application of appropriate programming voltages at the I/O pads, conducting paths can be established in such a way as to implement various logic functions.

Another new idea is illustrated in Figure 8 [Snider 04]. Complementary p-type and n-type transistors are formed at the crosspoints of a regular grid of metallic, p-type and n-type wires. Simulations indicate that defect-tolerant, PGLA-like circuits could be formed, even with defect rates as high as 10%.

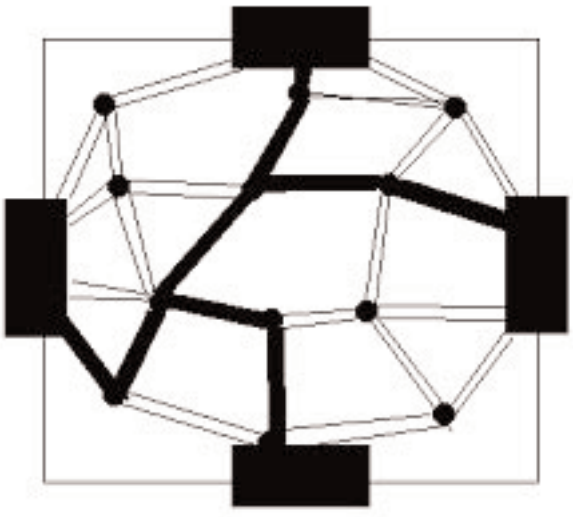

Figure 7. The Nanocell concept. Nanoparticles (black dots) are randomly deposited within the rectangular region, which has four input-output pads (black rectangles). Molecular wires are then deposited over the nanoparticles. Some of these will bridge pairs of nanoparticles, or nanoparticles and the I/O pads. Programming voltages are applied to selected pairs of pads to turn some of the molecule-particle contacts into negative-differential (NDR) switches. See [Husband 03] for details.

A different approach to fault tolerance, which still uses a large degree of structural regularity, is the NanoBox Processor Grid concept, which is based on regularly patterned, regularly organised, nested 'black boxes' containing error-correcting lookup tables. High levels of reliability, in the presence of large numbers of errors, are reported [KleinOsowski 04].

Yet again, another crossbar structure has been described in [Ziegler 03], where it is assumed that there willl be diodes at the crossbar junctions, with CMOS circuitry provided at the periphery of the structure to provide gain, circuit control, and I/O functions.

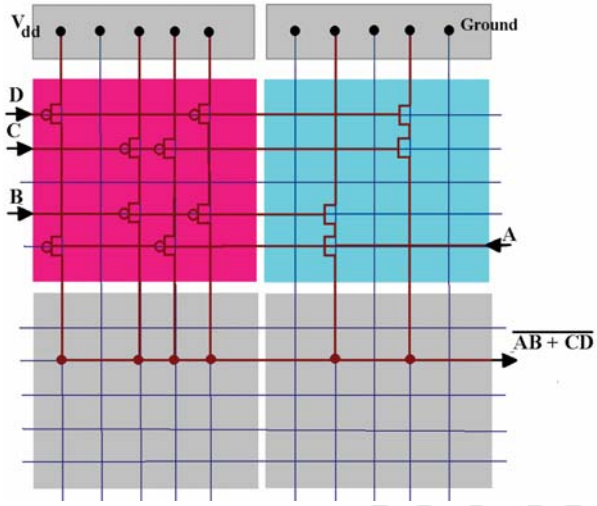

Figure 8. CMOS-like logic based on metallic wires (all horizontal wires), p-type wires (leftmost five vertical wires) and n-type wires (rightmost five wires), with p-type and n-type FETs formed at selected junctions. A chemical layer between the wire planes determines the type of device that can be formed at each junction. A typical separation between junctions might be 30 nm. Simulations suggest that the structure should provide defect-tolerant, reconfigurable PGLA-like circuits, even for device defect rates of ~10%. It is suggested that the circuit density could be 100 times higher than existing FPGAs (after [Snider 04]).

Another method for producing reliability in digital logic circuits is to use replicated 'neurons' in small feed-forward neural networks, whereby the thresholding operation of the network produces the desired Boolean output: the devices are not specified in detail [Schmid 03].

Although these ideas are interesting and potentially useful, it must be emphasised that almost in every case it is assumed that some device – typically a transistor – can be formed, with moderate reliability, where it is needed. These assumptions remain to be proved.

In almost every proposed nanosystem the concept of self-assembly appears, either explicitly or implicitly. It is assumed that methods exist (and sometimes this is true) for aligning nanoparticles or nanowires where they are required. An additional lower stratum of self-assembly is also needed – the nanoparticles or nanowires have themselves to be formed by self-assembly, preferably with extreme accuracy if undesirable variations in device properties are to be avoided. Much research and development is needed before these ideas can be fully verified.

What we have described above, albeit briefly, probably represents the main thrust of architectural (and circuit) development: regular, simple structures, where some degree of defective devices can be tolerated. Sometimes the thrust is towards neuromorphic architectures, sometimes it is directed towards PGLA-like structures.

There are in addition a number of other concepts which have been proposed, based on other technologies. Some of the most interesting of these are based on the use of DNA molecules. For example, by growing DNA tiles on a flat substrate, with the intermolecular contacts being directed by 'sticky' ends, Boolean operations such as cumulative XOR have been demonstrated, although the timescale (hours) and the reliability (~98.4%) suggest that scaling this mechanism up to much larger and faster systems will be difficult [Mao 00]. An interesting demonstration of DNA computing [Benenson 01] was the implementation in solution of a finite state automaton, with two ATP molecules being consumed at each step, with an energy loss of ~10^{-19} J, at a 'clock rate' of ~10^{9} Hz. There is, however, a long way to go before such systems would be economically viable. Other papers on this subject can be found in, for example, [Owenson 01].

Finally, and for completeness, we mention that in principle computing structures could be built using nanomechanical or microfluidic components, if they could be made small enough. A microfluidic processing structure with ~500 gates has been built and tested [Groismann 03].

6. Performance requirements

Most of the fundamental limits to the performance of conventional computing systems have been known for many years (e.g. Waser 03), but much work has yet to be carried out before these limits can be reached, and there are several factors whose effects are perhaps not widely known. Here we present just one simple example to illustrate how high-level and low-level factors combine to place restraints on the properties of nanodevices and nanoarchitectures if the ultimate computational limits are to be achieved.

Figure 9 is based on the assumptions of a hypothetical 1 cm^2 chip, working at 300K and containing 10^{12} nanodevices, The axes of the diagram are the mean power dissipation per cm^2 and the pulse duration: it is assumed that the mean switching probability is 10% for every device The symbol marked 'CMOS 2003' shows that, even if it were possible to pack 10^{12} present-day CMOS devices into an area of 1 cm^2 (which it is not!), then the power dissipation would be ~1 MW . Using the ITRS Roadmap estimates of future Si-based devices - the 'CMOS 2016' symbol – would only reduce the power dissipation by about a factor of 10. The horizontal line marked '100 Watts power dissipation per cm^2 ' represents a realistic estimate of the maximum allowable power dissipation per unit area (no matter what the device technology). The lower, dotted diagonal line marked '1kT for T = 300K' represents the thermal fluctuation limit – any system operating along this line will have *every one* of its devices failing approximately 50% of the time. The line marked '120kT' is a more practical limit: it corresponds to systems which have, on average, one device failing once per year. Only those systems whose power dissipation and pulse duration lie within the hatched region will have a better performance than systems based on present-day CMOS devices. In addition, only those systems which operate near the '120kT' black diagonal line will achieve the maximum theoretical performance. Such systems will have to use large amounts of parallelism.

The green diagonal lines, marked '30V, 3V….30mV' are the result of further constraints imposed by shot noise fluctuations, which are additional to thermal noise constraints. Briefly, shot noise can only be kept under control if each signal pulse contains at least 500 electrons. It can be shown (Forshaw 03) that if the practical thermal limit of ~120kT is to be approached, then shot noise control demands that the system operating voltage (V_{DD} in CMOS terminology) must be of the order of 30 mV or less.

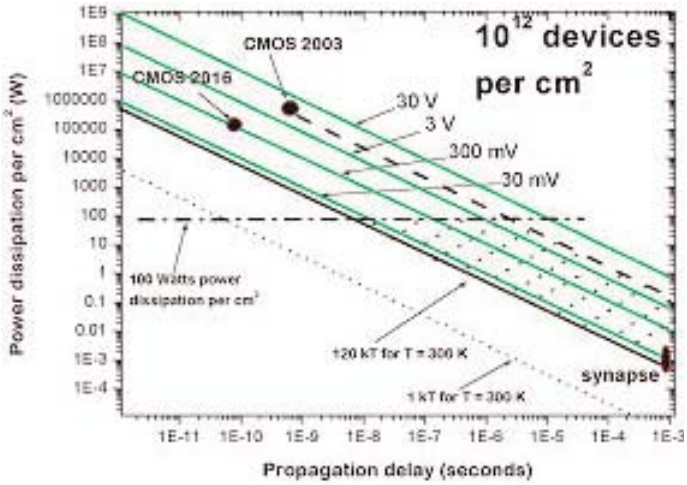

Figure 9. Plots of the maximum voltages (green diagonal lines), above which a system with 1012 devices per cm2 will fail catastrophically often, as a function of the pulse duration (or propagation delay per device) and the power dissipation per cm2. Devices in the hatched area will potentially have better performance than current CMOS devices, provided that system parallelism can be used to overcome their low operating frequency.

Much work remains to be done, to assess how best to achieve the maximum possible performance for a system with particular nanodevices, arranged in an appropriate nanoarchitecture, in order to implement a specific algorithm or set of algorithms.

7. Availability and training of human resources

Time constraints have prevented more than a token investigation into this topic, which was explored in detail in the follow-up study [NanoArch04]. However, it is clear that, while many European universities and research institutes (and indeed American and Pacific Rim establishments) are investing effort into nanotechnology in general, there are relatively fewer establishments that are investigating nanoelectronic systems in general, and even fewer who are explicitly including nanoarchitectural considerations in their research remit.

There are three obvious reasons for this. One is that the term 'nanotechnology' covers an enormous field, and 'nanoelectronics', although more restricted in its meaning, still covers a very wide range of research options. It is not financially possible, on a national or even supranational scale, to fund all of the possible research avenues. The second reason is that nanoarchitectural research has only recently been understood to have important practical implications for the development of nanoelectronic devices and systems. Thirdly, nanoarchitecture research, to be carried out successfully, requires a very wide range of multi-disciplinary skills, preferably in one individual, at the least in small active research groups. Such ideals are, alas, rarely achieved, but they must be aimed for, by appropriate training and development. There are signs that new device ideas are needed, because high-level architectural and system considerations suggest that many existing devices will fail to develop into useful systems. Responses to a questionnaire in an EC study [NanoArch04], and discussions with the correspondents, suggest that there is sufficient experience at an intermediate/high level to provide ade-

quate training in this area, although there is a shortage of well-trained European students. Summer schools, and possibly a focused network, would probably help provide the necessary increase in broad-based knowledge for research and development in this area.

Nanoelectronic architecture research, to be carried out successfully, requires a very wide range of multi-disciplinary skills, preferably in small active research groups.

8. CONCLUSIONS AND RECOMMENDATIONS

More or less every country in the EU is investing in nanotechnology research and development; many are investing in nanoelectronics; and one or two are thinking about investing in nanoarchitectures. It is the opinion of some workers that many currently-proposed or experimental nanodevices will not proceed beyond the research stage, and that those that do proceed to commercial production will be *complementary* to CMOS, rather than *replacements* for CMOS.

Any new or proposed nanoscale circuits or systems must first be assessed against a silicon CMOS benchmark. Some applications may need only small systems, some extremely large, but no nanoscale system will be successful unless it outperforms the Si benchmark in some way (cost, speed, size, etc.).

There is a large body of existing literature on architectural concepts, but new techniques continue to appear. The application of both old and new ideas to nanoelectronic systems has only just started.

Analysis tools for individual nanodevices exist, but with varying degrees of analytical approximation. Modelling tools for nanoscale circuits containing tens or hundreds of devices are as yet very primitive or nonexistent. At the system level, the effects of manufacturing defects or transient in-service errors will make very severe demands on the amount of circuit redundancy that will be needed for reliable operation: these constraints have yet to be analysed fully.

Much work remains to be done, to assess how best to approach the theoretical limits of performance for a system with particular nanodevices, arranged in an appropriate nanoarchitecture, in order to carry out a specific algorithm or set of algorithms. Nanoelectronic architecture research, to be carried out successfully, requires a very wide range of multi-disciplinary skills, preferably in one individual, at the least in small active research groups.

We suggest that the following actions would help in the future development of architectures for nanoelectronic systems:

A rigorous investigation should be made, where possible, into which existing or proposed nanodevices will provide better performance in the future than CMOS-related devices, when assembled onto high-density chips (i.e. with more than ~10^{10} devices). The analysis should be divided into three categories, namely logic, memory, and CMOS-complementary systems (e.g. sensors, optical interfaces, SoC).

For devices where sufficient information may not be available (e.g. molecular-scale or CNT devices), the funding of research should continue, to allow their performance to be assessed.

More attempts should be made to fabricate small 'circuit-level' systems, where several devices and input-output structures are combined at a true nano-scale.

The fabrication of such small systems should be done in combination with analysis/simulation of the behaviour of these structures. This quasi-mesoscopic region, where quantum mechanical coherence and decoherence phenomena overlap with classical effects (capacitative coupling, thermal fluctuations) is extremely difficult to analyse properly, but the development of molecular-scale devices and systems will depend on the availability of adequate modelling tools.

It is becoming increasingly likely that there will be a divergence between systems that are based on more-or-less conventional digital logic, where 100% reliability is desired, and systems (notably for pattern recognition of various kinds) where analogue/probabilistic principles are involved and less than 100% reliability is acceptable. At present such 'soft' systems are almost exclusively implemented as software running on conventional computers. It is possible that some nanoscale devices/systems will be intrinsically analogue/probabilistic in nature, and/or be prone to errors which would make them unsuitable for digital logic applications. More efforts should therefore be made to see if such 'soft' systems will offer any better performance than CMOS-based systems. These soft systems might be nanoelectronic in nature, or nanophotonic, or perhaps some combination of these with sensors.

'Blue sky' research into new nanodevices/systems should be encouraged, to improve the chances of reaching the ultimate performance limits of conventional and/or analogue computing.

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Figure 3 and some of the material in the Conclusions section are from the follow-on study (Nano_Arch_Review, EC FP6/2002/IST/1 Contract No 507519)

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Footnote: It must be emphasised that the contents of this report represent the personal views of the authors. Because of the report's brevity, many topics receive no more than a mention: this should in no way be taken to be an indication of the relative importance of such topics. Due to time constraints, only a small number of references are provided: please contact the authors if individual references are needed.

ANNOUNCEMENT

NID 16 Workshop. 22 - 24 June, 2005 (Glasgow, UK)

The NID 16 Workshop will be organised by the **University of Glasgow** in collaboration with the **European Commission (IST/FET/Nano)** and the **PHANTOMS Foundation.**

The Workshop will be held in Glasgow, one of the most magnificent "Victorian" cities in the world and only a short journey from Scotland's scenic west coast.

The NID 16 workshop will gather participants from several projects funded by the NID pro-active initiative (part of the European Union's IST research programme). There will be a Plenary session during which presentations from the EU projects under review and invited talks from experts outside the NID initiative will be given. There will also be working group sessions focused on the application of a broad range of nano-scale technologies such as information processing and on the prospects for replacing mainstream approaches, such as CMOS.

See more information about this event at http://www.phantomsnet.net/nidconference10/

Life beyond CMOS

"For the last 40 years computers have been getting faster as CMOS chips have become smaller, faster and cheaper. But all good things come to an end and, all around the world, people have begun looking at alternative electronic devices that might follow on from CMOS."

So said Dr Michael Forshaw, coordinator of IST project **ESCHER**, who gathered with other researchers to present recent findings in the search for new technology to succeed CMOS (complementary metal oxide semiconductors), during the 15th Nanotechnology Information Devices (NID) Workshop, organised by the **PHANTOMS Foundation** based in Madrid.

CMOS has been the dominant chip technology used by the world's electronics industry for several decades. CMOS semiconductors use both negative and positive polarity circuits. Since only one of the circuit types is on at any given time, CMOS chips require much less power than chips using just one type of transistor. This makes them particularly attractive for use in battery-powered devices, such as portable computers.

Getting smaller
Since their introduction, CMOS transistors have shrunk exponentially in size in accordance with Moore's Law. This law predicts a doubling of transistors per integrated circuit every 18 months. However, the ability to scale down CMOS further appears to be reaching physical and technical limits. The International Technology Roadmap for Semiconductors (ITRS), a worldwide organisation responsible for identifying the technological challenges and needs facing the semiconductor industry, predicts the size limit for CMOS technology to be 5 to 10 nm. Furthermore, ITRS believes this limit will be reached in 15-20 years time.

Semiconductor industries such as Intel in the US and Infineon, STMicroelectronics and Philips in Europe are now developing the factories for CMOS chips with 65 nm size features, the `65 nm node´, which ITRS foresees in full production in 2007. To meet future needs of the electronics industry, ITRS has set semiconductor manufacturers the target of producing 45 nm CMOS technology nodes, or junctions, by 2010. However, to manufacture CMOS technology below 65 nm, new fabrication treatments are needed. "The problem with conventional thermal treatments," explained Dr Vittorio Privitera of Consiglio Nazionale delle Ricerche (CNR), "is it is not possible any more to achieve the junction depths and the special characteristics of the dopant layer that are required."

Privitera is the coordinator of the **FLASH** project, which has been developing a new laser-based treatment, called excimer laser annealing (ELA), to meet the ITRS target. Initial results have been extremely encouraging. "The laser is able to make ultra-shallow junctions with dopant profiles which are extremely sharp and electrically very active. This is the first time that this has been done," reported Privitera. Over the course of 2005, Privitera and his partners intend to construct and evaluate a prototype production line for fabricating MOSFET transistors using the new method.

Recently completed project **NEAR** was also at the workshop. NEAR aimed at developing new non-CMOS nanoelectronic devices that are extremely compact, consume low power and operate at room temperature. Two component types were investigated, known as Three Terminal Ballistic Junction (TBJ) devices and Self Switching Devices (SSD). During the project, basic logic circuits were created using TBJ and SSD devices, and successfully operated at room temperature.

Looking to the future
Discussing future directions in mono-molecular electronics, the name given to digital logic circuits designed using single molecules, Dr Christian Joachim, a Research Director at the Centre National de la Recherche Scientifique (CNRS) and **CHIC** project partner, described the majority view that: "We have decided to take a bottom-up approach, starting with atoms and asking ourselves 'what do we need?' or 'what is the minimum sized molecule to implant a computation inside it?'" Amongst the key issues to be tackled are: what computing resources are available, how information can be exchanged internally, and what cooling and energy requirements there are.

Another area covered at the event was alternative electronics, investigating devices that could replace CMOS beyond the 10 to 5 nm frontier and provide at least comparable performance whilst requiring less power and lower fabrication costs. Dr Arianna Filoramo, a researcher at CEA-Saclay and **SATURN** project partner, explained how current research is looking into areas such as the fabrication and characterisation of low dimensional materials such as nanowires, nanotubes and nanodots; new methods of fabricating nanodevices such as self-assembly and molecular lego; as well as new architecture paradigms for nanodevices.

A third strand was nano-electro-mechanical systems (NEMS). Said Professor Jürgen Brugger of Ecole Polytechnique Fédérale de Lausanne (EPFL): "I would like to emphasise the 'm' in nano-electro-mechanical systems. We are really focussing on the mechanical aspects of nanodevices." The identified challenges being tackled included nanoscale mechanics, fabrication techniques for NEMS elements, detection methods and interfacing of NEMS.

The broad spectrum of discussions that took place at the NID Workshop served to show that the semiconductor industry is entering an exciting, if uncertain, period. The expected physical challenges of advancing CMOS technology is creating a flurry of activity which is leading to a wide range of potential technical successors. Technology fragmentation means there will be a tremendous opportunity for the industry to differentiate and so add value, supported by researchers such as those at the NID Workshop.

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NID Working Group on Mono-Molecular Electronics

Coordinators: C. Joachim and G. Meyer
3rd meeting, February the 1st, 2005

This 3rd meeting focussed on architecture problem. The central question on the stage was: for molecular electronics, will it be necessary to remain at the single molecule = one device challenge or do we need to explore more how a single molecule, of course more complex can perform more than a simple amplification, rectifier or rectifier action. Of course, there are a lot of architectural options to be explored ranging from forcing the molecule to have the topology of a miniaturized electronic circuit to the use of quantum intramolecular non-stationnary time evolution to perform a logic function. The important point here is not to be restricted to a given technology but to provide new ways to design an ultra-small piece of material to compute.

Agenda	
15:00 – 15:15	**C. Joachim**: *M2e Presentation, Scope and Goals*
15:15 – 15:30	**D.Guedj**: *Atom-Based Technologies?*
15:30 – 16:00	**F. Remacle**: *Towards Molecular Logic Machines Using Inter- and Intra-Moelcular Dynamics*
16:00 – 16:30	**C. Joachim**: *What Kind of Mono-Molecular Electronics: Architecture, Technology & Chemistry?*
16:30 – 17:00	**Discussion & Conclusions**

All the technological aspect ranging from imaging, interconnection at the atomic scale to chemistry have already been explored in the previous meeting. But D. Guedj from the Commission started from a short presentation on how the field of Molecular electronic is on demand of atomic scale technology and that this demand is also very present in other fields like the cold atom trap and molecular scale nanobiotechnology. Of course, the requirements in each case are a bit different, but there is a net convergence of techniques and goal which would requires a co-ordinating action in preparation of the 7th Framework Programme. The way such coordination action can be put in action was discussed in relation with the 6th Framework Programme project recently accepted or in negotiation at the IST level.

The second presentation was given by F. Remacle from the Department of Chemistry (University of Liege). She had presented concrete examples, up to the level of a full adder, of concatenated logic gates that are operated on different parts of a molecule or on different molecules that are coupled. The proposed scheme uses the (optical) excitation of molecular levels and their intramolecular and intermolecular dynamics to connect several logic gates. We will then show that it is possible to implement finite state and Turing machines at the molecular level optically using the dynamics of a 3 level quantum system. Finally, an implementation of a search algorithm by chemical kinetics was discussed. Questions from the audience were dealing with the statistical behaviour of the through space energy transfer process required to concatenate the elementary logic function. Electrically driving the inputs was also discussed in particular in relation with STM like electrochemistry experiments which seems well adapted to the computational scheme presented by F. Remacle.

The third presentation was given by C. Joachim from the Nanoscience group of CEMES/CNRS (Toulouse). He had presented the principle of a new intramolecular logic gate design called Quantum Hamiltonian Computing. Using an intramolecular single electron transfer process, it was shown how computing inside a quantum system can be performed using the time evolution driven by the preparation of the system in a non-stationary state. The molecule Hamiltonian is separated in three parts: the input, calculation, and output parts. Two optimisation procedures were described in order to design an efficient mono-electronics level structure for molecular logic gates. An XOR gate and a half-adder using six electronic quantum levels were presented. A dinitro[1,3]anthracene molecule was described, performing an fi adder logic function with no resemblance to the topology of an electronic circuit performing the same function. The logic function is obtained by the control of the molecule quantum trajectory in its p molecular orbitals electronic quantum state space by changing the conformation of the nitro groups, starting from an initial non-stationary state independent of the input configuration. Questions arise from the audience about the practical way to program the input status and to read out the results.

The final discussion conclude that there is a lot of quantum resources inside a single molecule to embed a complex logic function. But a lot of progresses remain to be done in a new atomic scale technology to have access to those resources.

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1st NEMS Working Group

Coordination: J. Brugger (EPFL) and Francesc Perez-Murano (CNM)

The scope of the NEMS Working Group (WG) is to create a forum for those in Europe interested in the creation of new nano-electro-mechanical devices and systems. This WG will be based on activities like seminars during the NID meetings, tutorials on a specific topic and the building of roadmaps in nanomechatronics for the information industry. The basic idea is to bring together researchers working on specific topics in the emerging field of nano-electro-mechanical systems (NEMS).

The following topics will be covered by the NEMS WG:

Mechanics at nanoscale
Fabrication techniques for NEMS elements
Detection methods, interfacing of NEMS
Links to life-sciences
Roadmaping: opportunities, risks and barriers

Below, we provide a preliminary list of European Groups working in NEMS research areas who expressed their interest in being involved in the WG activities.

Collection of members input

Ernst Meyer, University of Basel (CH)
Laslo Forró, Andrzej Kulik; IPMC, Ecole Polytechnique Federale de Lausanne (CH)
Juergen Brugger, LMIS, Ecole Polytechnique Federale de Lausanne (CH)
Mat Jonson, Gothenburg University (S)
Stephen Purcell, LPMCN (F)
Gabriel Abadal, ETSE-UAB (E)
Herre van der Zant, TU-Delft MED (NL)
Jari Kinaret, Chalmers University (S)
Felix von Oppen, FU Berlin (D)
Francesc Perez-Murano, CNM-CSIC (E)
Jan Lichtenberg, ETH Zurich (CH)
Bioprobes : Zachary Davis, Nanointegration : Peter Boggild, Kristian Molhave, MIC (DK)
Joerg P. Kotthaus, LMU Muenchen (D)
Liesbet Lagae, Wim van Roy, IMEC-MCP (B)
Urs Sennhause, Philipp M. Nellen, EMPA (CH)

Group / Name: University of Basel / Ernst Meyer
Activity: MEMS/NEMS
Core competences:
Nanotribology
Development of scanning probe microscopy
Cantilever-based sensors
Chemical analysis on the local scale
Equipment
Ultrahigh vacuum force microscopy
magnetic resonance force microscopy
sensors for biology and chemistry
Combination of TOF and AFM
Interest in collaboration
Control of friction of NEMS-devices
Sensors for ultimate force and stress sensitivity
Probe microscopy for local chemical analysis

Group / Name: EPFL-IPMC / Laslo Forró, Andrzej Kulik
Activity: biostructures & nanomechanics
Core competences:
Quantitative nanoscale measurements
nanomechanics of mesoscopic objects
adhesion, nanotribology, molecular recognition
nanomanipulation, nanolithography
Scanning Probe Microscopy, nanoindentation
Equipment:
six AFM's with lot of optionsAFM-based nanomanipulator (NanoFeel)
Photonic Force Microscope
Scanning nanoindenter (Hysitron)
Interest in collaboration:
Yes (t.b.d.)

Group / Name: EPFL-LMIS1 / Juergen Brugger
Activity: MEMS/NEMS
Core competences:
Micro-nano integration
Nanopatterning
Scanning probes
Nanostencil
Nanomembranes
Equipment:
Clean-room facilities
Focused ion beam
Silicon / polymer processing
Materials characterization facilities
Interest in collaboration:
Parallel, large-scale, reliable NEMS device fabrication
Integration and characterization of NEMS

Group / Name: Gothenburg University
Activity: Theoretical and experimental study of carbon-based NEMS
Core competences:
Theoretical modeling of nanoelectromechanical devices
Experimental studies of carbon nanotube NEMS (nanorelay)
Development of CMOS-compatible materials and processes for integration of CVD-grown carbon nanotubes in a silicon environment
Equipment:
Carbon nanotube growth equipment (CVD, plasma CVD), micro-Raman. Access to large modern clean room with extensive equipment
Interest in collaboration:

Group / Name: LPMCN/Stephen Purcell
Activity: Nanotubes/Field emission
Core competences:
Nanotube growth
Field emission electron sources
Field emission ion sources
Equipment:
Ultra high vacuum
CVD, PECVD growth
Materials characterization facilities
Interest in collaboration:
t.b.d. (nanomechanics of nanotubes and nanowires)

Group / Name: Electronic Circuits and Systems (ECAS) ETSE-UAB / Gabriel Abadal
Activity: CMOS integrated MEMS and NEMS design and characterization
Core competences:
MEMS/NEMS transducer electromechanical modelization
Co-simulation of MEMS/NEMS transducers integrated with CMOS cicuitry
Electrical and functional characterization of MEMS/NEMS
Equipment:
Simulation software for circuitry and MEMS/NEMS
Probe station for low frequency and RF MEMS/NEMS
Interest in collaboration:
Bio and RF applications groups
MEMS-NEMS fabrication groups

Group / Name: TUD-MED / Herre van der Zant
Activity: NEMS
Core competences:
Bottom-up and top-down fabrication
suspended carbon nanotubes
suspended nanowires
HR e-beam lithography, incl. opt. mask making
advanced plasma processing (dry etching)
transport measurements
quantum theory of NEMS
Equipment:
Fully equipped fabrication facilities in cleanroom class 10000 environment*
TEM, Dual beam (FIB/SEM)
low-noise measurements at low temp. (including high frequencies)
Interest in collaboration:
(new) detection methods
(new) materials
modeling

* including:
- e-beam & optical litho,
- wet processing,
- dry etching (RIE, ICP, ECR; F and Cl chemistries),
- deposition (evaporation, sputtering; metals, IVsemiconductors, dielectrics),
- thermal processing (RTA, furnace),
- Inspection (SEM, opt. microsc., ellipsometry, AFM/STM)

Group / Name: Chalmers University of Technology
Activity: Theoretical and experimental study of carbon-based NEMS
Core competences:
Theoretical modeling of nanoelectromechanical devices
Experimental studies of transport through individual molecules bridging nanogaps between metal electrodes
Development of CMOS-compatible materials and processes for integration of CVD-grown carbon nanotubes in a silicon environment
Equipment:
Large modern clean room with extensive equipment
Interest in collaboration:

Group / Name: Felix von Oppen (Freie Universität Berlin)
Activity:
Theory of quantum transport in nanoscopic systems
Core competences:
Modelling of electronic transport through nanoelectromechanical systems
Equipment:
Interest in collaboration:

Group / Name: CNM-CSIC/ Francesc Pérez-Murano
Activity: Micro&nano fabrication/ NEMS/Detection methods, interfacing of NEMS/NEMS on CMOS

Core competences:
Micro/nano integration
Micro/nano fabrication
CMOS/NEMS integration
Nanomechanical sensors
HF mechanical resonators
Equipment:
Clean room facilities for micro and nano fabrication, including CMOS circuit fabrication and nanofabrication equipment
Interest in collaboration:
t.b.d.

Group / Name: ETH Zurich/PEL / Jan Lichtenberg
Activity: CMOS-integrated MEMS and NEMS
Core competences:
Cantilever probes for chemical sensing
Cantilever probes for surface scanning
Integration of MEMS/NEMS with dedicated CMOS electronics
MEMS packaging
Micro- and Nanofluidics
Equipment:
Clean-room facilities
Silicon / polymer processing
Microelectronics and MEMS design and simulation
Access to commercial CMOS foundries
Microfluidics laboratory
Interest in collaboration:
Project partner for cantilever-based sensing and surface-scanning systems, microfluidics for single-cell and -molecule handling and analysis

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Group / Name: BioProbes (Zachary Davis)
Activity: Micro/nano based probe sensors for bio/chemical applications
Core competences:
Nanocantilevers sensors
CMOS integration with MEMS/NEMS
Piezoresistive probe sensors (Si)
Plastic based probe sensors (SU-8)
Nanotube based sensors
Equipment:
Clean-room facilities
High end e-beam facility
Nano-imprint
Material characterization
Plastic processing
Interest in collaboration:
yes (t.b.d.)

Group / Name: LMU München - nanophysics group / Jörg P. Kotthaus
Activity: NEMS
Core competences:
Nanofabrication methods
Nanotweezers
Nanomechanical charge transport,
single electron shuttle
Low-dimensional electron systems in free-standing nanostructures
Nano-opto-mechanical systems
Equipment:
cleanroom facilities
electron beam lithography
Si, GaAs and carbon nanotube processing technology
Interest in collaboration:
Nanowire growth,
Theoretical models

Group / Name: IMEC-MCP/NEXT-ART Liesbet Lagae (Wim Van Roy)
Activity: Magneto-electronics/NEMS
Core competences:
Micro-Nano integration
Materials research (III-V heterostructures, nitrides, Poly-SiGe, Diamond, ferromagnetic metallic thin films, magnetic semiconductors)
Magnetization and spin dynamics, magnetostriction [1]
Scanning Hall Probe Microscopy [2,3]
Surface functionalisation [4]
NEMS resonators (recently started) [5]
Equipment:
Fully equipped clean room facilities for Si, III-V, magnetic materials, etc…
Material deposition (MBE, sputtering, PLD) and characterization
(Magnetic) characterization with special expertise in high frequency, time-resolved, optical and magneto-motive measurements
AFM, STM, Scanning Hall Probe Microscope
Interest in collaboration:
Yes, preferably in the form of a Network (RTN or NoE).
new detection methods
dissipation mechanisms
sensors for ultimate sensitivity

Group / Name: Nanointegration group at MIC, DTU Peter Bøggild / Kristian Mølhave
Activity: Nanotube and nanowire integration in MEMS systems.
Core competences:
Cantilever microchips
Micro 4 point probes
Electrostatic grippers
Grippers with force feedback
Piezo resisitive force sensors
Waferscale dielectrophoretic assembly of nanodevices
In-situ SEM nanomanipulation
Equipment:
1000 m^2 Cleanroom facility (incl. waferscale EBL, with Danchip, DTU)
In-situ SEM nanomanipulation systems
Optical nanomanipulation systems with controlled humidity.
TEM (with A. Horsewell, IPL, DTU)
Epitaxial nanowire growth (with L. Samuelson, Lund university)
Carbon nanotube growth (with B. Milne, Cambridge)
Environmental electron beam deposition (with C. Persson, Lund university)
AFM and UHV-STM starting up
Interest in collaboration:
Applications of nanowires and nanotubes in functional devices
Functionalization of nanowires and tubes
Application of nanomanipulation

Group / Name: Empa, Electronics/Metrology Laboratory, Reliability Center, Dr. Urs Sennhauser (head), Dr. Philipp M. Nellen
Activity:
Physical modelling and simulations in the field of reliability, safety and security of materials, devices and systems
Developing sensors and measurement devices (electronics / photonics)
Micro- and nanotechnology
Core competences:
Equipment:
Reliability testing facilities
Materials characterization facilities at Empa (SEM, ESEM, AFM, STM, TEM, TOF-SIMS, and others)
2 Focused-Ion-Beam (FIB), optical full field methods and X-ray microtomography at Empa and at the synchrotron light source SLS/PSI,
Interest in collaboration:
Fabrication, Modification, 3D Structuring, Characterization of M(O)EMS with FIB and related tools
Reliability analysis of nanosystems including packaging

Conductive tips for atomic force microscopy (May 24, 2005)

Researchers in Switzerland have tested an atomic force microscope with an electrically insulated conductive tip. The scientists, from the University of Basel and University of Neuchâtel, imaged the hexagonally packed intermediate layer of the red bacterium Deinococcus radiodurans.
http://www.nanotechweb.org/articles/news/4/5/12/1

Dots for data storage (May 19, 2005)

Physicists in the US and Germany have reported on a new way to double the storage capacity of magnetic recording devices. The method, which is compatible with standard lithography fabrication techniques, could help overcome the limits of conventional magnetic recording and allow storage densities of 1 terabit (1012) bits per square inch (M Albrecht et al. 2005 J. Appl. Phys. 97 103910). The increase in storage capacity is made possible by combining arrays of magnetic dots with multiple magnetic layers.
http://physicsweb.org/articles/news/9/5/12/1

Motorola Labs Debuts First Ever Nano Emissive Flat Screen Display Prototype (May 09, 2005)

Building Upon Carbon Nanotube Technology, Motorola Prepares to Revolutionize the Flat Panel Display Industry
http://www.motorola.com/mediacenter/news/detail/0,,5484_5474_23,00.html

Nanostructures branch out with templates (May 05, 2005)

Researchers at Rensselaer Polytechnic Institute, US, have used ceramic templates to produce hierarchically branched nanowires and nanotubes for the first time. The team grew carbon nanotubes and metallic nanowires inside anodic aluminium oxide structures.
http://www.nanotechweb.org/articles/news/4/5/3/1

Harvard scientists create high-speed integrated nanowire circuits (April 27, 2005)

Chemists and engineers at Harvard University have made robust circuits from minuscule nanowires that align themselves on a chip of glass during low-temperature fabrication, creating rudimentary electronic devices that offer solid performance without high-temperature production or high-priced silicon.
http://www.eurekalert.org/pub_releases/2005-04/hu-hsc042705.php

GDR-E and Phantoms Foundation initiated Strategic Partnership in Nanotubes (2005-04-28)

The GDR-E (European Group of Research on the Science and Applications of Nanotubes) has become a Strategic Partner of the Phantoms Foundation, non-profit organisation based in Madrid (Spain).
This collaboration will start with the organisation by the GDR-E section on “Nanoelectronics and Field Emission” of a session entitled “Carbon Nanotubes Based Nanoelectronics and Field Emission” at the upcoming Trend in NanoTechnology (TNT2005) International Conference Series.
http://dbs.cordis.lu/cordis-cgi/srchidadb?ACTION=D&SESSION=128282005-5-6&DOC=4&TBL=EN_RTDN&RCN=EN_RCN_ID:3036&CALLER=CORDISwire

Innovative Fountain Pen Writes On The Nanoscale (April 27, 2005)

Researchers at Northwestern University have demonstrated writing at the sub-100 nanometer molecular scale in fountain-pen fashion. They developed a novel atomic force microscope (AFM) probe chip with an integrated microfluidic system for capillary feeding of molecular ink.
http://www.sciencedaily.com/releases/2005/04/050427133843.htm

New polymers for applications in nanopatterning and nanolithography (April 19, 2005)

The Cidetec Technological Centre continues to invest in nanotechnology development with its participation in the European NAPA (Emerging Nanopatterning Methods) project. The research institution is directing a working subgroup to develop new thermoplastic polymers for applications in nanopatterning and nanolithography.
http://www.physorg.com/news3785.html

The impact of its environment on a quantum computer (April 14, 2005)

Scientists have discovered how the performance of a quantum computer can be affected by its surrounding environment. The study, published in the latest issue of the journal Science, will help engineers to better understand how to integrate quantum components into a standard office computer - moving us one step closer to a future of quantum computing.
http://www.physorg.com/news3726.html

New material structure produces world's fastest transistor (April 11, 2005)

A new type of transistor structure, invented by scientists at the University of Illinois at Urbana-Champaign, has broken the 600 gigahertz speed barrier. The goal of a terahertz transistor for high-speed computing and communications applications could now be within reach.
http://www.physorg.com/news3662.html

X Architecture Becomes Mainstream (April 01, 2005)

Using diagonal interconnects on Metal 4 and above, X Architecture can produce chips with 20% less interconnect and 30% fewer vias. That results in a more efficient chip than possible with the orthogonal Manhattan configuration, while maintaining IP compatibility on Metal 1 to 3 and preserving existing infrastructure.
http://www.reed-electronics.com/semiconductor/article/CA513393?pubdate=4_1_2005

Molecular Memories: A Low-Cost Alternative? (April 01, 2005)

Since the 1980s, molecular electronics has been the focus of much conjecture and an increasing amount of research (now largely grouped as part of the massive nanotechnology effort). Great potential was seen for organic materials such as proteins to act as switches, much like transistors do today. It was theorized that fields of protein-based memories could be grown, making silicon obsolete.
http://www.reed-electronics.com/semiconductor/article/CA513373?pubdate=4%2F1%2F2005&industryid=3028

New look for nanomotors (March 23, 2005)

Physicists in the US have built the first nanoelectromechanical device that exploits the effects of surface tension. The "relaxation oscillator" consists of two droplets of liquid metal on a substrate made of carbon nanotubes and can be controlled with a small applied electric field. Alex Zettl and colleagues at the University of California at Berkeley and the Lawrence Berkeley National Laboratory say the device could find use in various nanomechanical applications, including actuators and motors (B C Regan et al. 2005 Appl. Phys. Lett. 86 123119).
http://www.nanotechweb.org/articles/news/4/3/11/1

Moore says nanoelectronics face tough challenges (March 09, 2005)

Although many believe the future of the computing industry lies with building chips out of carbon nanotubes or other novel materials, Intel co-founder Gordon Moore predicts it won't be easy to replace silicon.
http://news.zdnet.com/2100-9584_22-5607422.html

(June 2005)

Nanomaterials and Nanotechnologies
Greece (14 - 18 June, 2005)
http://www.ipme.ru/ipme/conf/NN2005/

BaCaTec Summer School: Semiconductor Nanophotonics - Technologies, Physics, Applications
Germany (26 June - 01 July, 2005)
http://www.physiscs.uni-wuerzburg.de

NT05: Sixth International Conference on the Science and Applications of Nanotubes
Sweden (26 June - 01 July, 2005)
http://nanotube.msu.edu/nt05/

8th International Conference on Nanometer-Scale Science & Technology (NANO-8)
Italy (28 June – 02 July, 2005)
http://www.nano8.org/

(July 2005)

MSED 2005 Workshop on Modeling and Simulation of Electron Devices
Italy (04 – 05 July, 2005)
http://holden.iet.unipi.it/msed/

8th International Conference on the Structure of Surfaces (ICSOS8)
Germany (18 – 22 July, 2005)
http://www.icsos8.uni-muenchen.de/

(August 2005)

8th International Conference on Non-Contact Atomic Force Microscopy
Germany (15 – 18 August, 2005)
http://www.ncafm.info/

ESONNS: European School on Nanoscience and Nanotechnologies
France (21 August - 09 September, 2005)
http://www.esonn.inpg.fr

Trends in Nanotechnology TNT2005
Spain (29 August – 02 September, 2005)
http://www.tnt2005.org

EMAG - NANO 05 Imaging, Analysis and Fabrication on the Nanoscale
United Kingdom (31 August – 02 September, 2005)
http://conferences.iop.org/EMNA/

(September 2005)

ECOSS23: European Conference on Surface Science
Germany (04 - 09 September, 2005)
http://www.physiscs.fu-berlin.de/ecoss

MNE2005 - International Conference on Micro- and Nano-engineering
Austria (19 – 22 September, 2005)
http://www.mne05.org/

Postdoctoral Position in Heterogeneus Catalysis

One year post-doctoral position in the R&D division at Haldor Topsoe A/S (near Copenhagen, Denmark; see also www.topsoe.com). The successful applicant should have a Ph.D. in chemistry, physics or a related field. Experience within one or more of the fields of catalysis, TEM or surface science would be an advantage.

For further information please contact
Dr. A.M. Molenbroek Haldor Topsoe A/S,
e-mail: am@topsoe.dk
tel: +45 4527 2483

ALBA has started the selection procedure in order to hire scientists for the beamlines to be built in the first phase.

The successful candidates will be expected to have the responsibility (in total or in part) for the design, construction and operation of the beamlines together with the development of an in-house research program. Indefinite and fixed term contracts will be considered depending on the experience and circumstances of the applicants. The evolution from fixed term contracts to indefinite ones will also be contemplated.

If you are interested in being considered for such positions, please send your CV and a letter describing your interests, experience and boundary conditions to yolanda.ruiz@cells.es before 1st September 2005.

Open Post-doc position in AFM applications to Biology at the Nanobioengineering Laboratory (Parc Cientific de Barcelona)

The Nanobioengineering Laboratory offers a post-doc position for 1+1 years in the field of Atomic Force Microscopy in Biology to start as soon as possible. The successfull candidate will work in the framework of two European projects on Nanobiotechnology (SPOTNOSED and CELLPROM), and will have acces to the most advanced nanobiotechnology facilities in one of the best nanobiotechnology laboratories in Spain.

Candidates interested, please send your application material including a cover letter with a resume to Prof. Josep Samitier (jsamitier@pcb.ub.es), with a copy to Dr. Gabriel Gomila (ggomila@pcb.ub.es)

PhD Position Available

Starting date: October 1, 2005
Applicants should have a university degree in Physics, Electronic Engineering, Chemistry or equivalent knowledge. Candidates with a strong background in physics, microelectronics, and chemistry are encouraged to apply.

Position : Fabrication and physical investigation of nanometer sized memories based on Silicon nanowire and organic molecules (Molecular NanoFlash)

For further information about the position, please contact:
B. De Salvo, CEA/LETI/D2NT/LNDE
17, rue des Martyrs, 38054 Grenoble
Tel. : 04.38.78.64.97, Fax. : 04.38.78.94.56
e-mail: bdesalvo@sorbier.cea.fr

Postdoc: Atomic Scale Modeling of Insulators At Chemnitz Technical University

Job description: Atomic Scale Modeling is reaching industry! Do you want to apply your knowledge to industrial applications?
Our group has open postdoc positions in the area of ab-initio based computations of semiconductor/ insulator interfaces, defect states in insulators, high-k materials and tunneling through MOSFET structures on the base of TDDFT, GW, etc. codes.
Applicants with good programming abilities in C and FORTRAN, knowledge in simulation techniques and ab-initio DFT-like computation are welcome to apply for the positions. Applications including a CV, a list of publications and 3 letters of recommendations should be send as soon as possible. The applicants should be able to start not later than the 1st of July 2005. Because of our time constrains and long time needed to issue a EU Visa, we prefer applicants from EU.

Contact: Dr. E. P. Nakhmedov E-mail: opto@etit.tu-chemnitz.de
Fax: +49-371-531-3004
Tel: +49-371-531-3080

EUROPEAN SCIENTIFIC PORTALS

Community Research & Development Information Service (CORDIS):
http://www.cordis.lu

CORDIS Wire (Press-Releases):
http://www.cordis.lu/wire/

Activities of the European Union - Research and Innovation:
http://europa.eu.int/pol/rd/index_en.htm

FP6 RESOURCES

Six Framework Programme (FP6):
http://fp6.cordis.lu/fp6/home.cfm

Information Society Technologies (IST):
http://www.cordis.lu/ist/

Future and Emerging Technologies (FET):
http://www.cordis.lu/ist/fet/

FET Newsletter (Issue n.1):
ftp://ftp.cordis.lu/pub/ist/docs/fet/nl-1.pdf

Emerging Nanoelectronics (NID-Proactive Initiative):
http://www.cordis.lu/ist/fet/nid.htm

Nanotechnologies and Nanosciences (NMP):
http://www.cordis.lu/nmp/home.html

Find an FP6 call:
http://fp6.cordis.lu/fp6/calls.cfm

Find an FP6 project:
http://www.cordis.lu/fp6/projects.htm

INCO info point on international co-operation activities:
http://www.cordis.lu/fp6/inco.htm

Nanotechnology Service of the European Commission:
http://www.cordis.lu/nanotechnology/

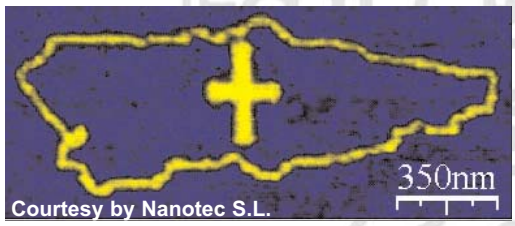
FP7 RESOURCES

Towards FP7: gateway to the preparation of the Seventh Framework Programme (FP7):
http://www.cordis.lu/fp7/

Technology Platforms:
http://www.cordis.lu/technology-platforms/home.html

Europa - Investing in our future:
http://europa.eu.int/comm/financial_perspective/index_en.htm

TNT2005 Trends in NanoTechnology



The sixth edition of the **Trends in Nanotechnology International Conference Series (http://www.tnt2005.org)** will be held in Oviedo (Spain) from 29 August to 02 September, 2005.

This event is organised by the following institutions:

CEA/LETI/DRFMC (France)

Consejo Superior de Investigaciones Científicas (Spain)

Donostia International Physics Center (Spain)

Georgia University of Technology (USA)

NIMS Nanomaterials Laboratory (Japan)

PHANTOMS Foundation (Spain)

Purdue University (USA)

Universidad Autonoma de Madrid (Spain)

Universidad Carlos III (Spain)

Universidad Complutense de Madrid (Spain)

Universidad de Oviedo (Spain)

MAJOR TOPICS

The TNT presentations (keynotes, orals & posters) are categorised within the following topics:

Carbon Nanotubes Based Nanoelectronics and Field Emission
Nanostructured and Nanoparticle Based Materials
Low-Dimensional Materials (Nanowires, Clusters, Quantum Dots, etc.)
Nanofabrication Tools and Nanoscale Integration
Nanochemistry
Nanobiotechnologies
Theory and Modelling at the Nanoscale
Nanomagnetism and Spintronics
Scanning Probes Methods
Ultimate Limits of Measurement: Metrology and Nanostandards

Since the first event (TNT2000) launched in Toledo (Spain) by Dr. Antonio Correia and Prof. Pedro A. Serena, the series of conference Trends in Nanotechnology has become a yearly key meeting point for Nanotechnology and Nanoscience scientists around the world.

Since its infancy, the core of the Organising Committee is composed by Dr. Antonio Correia, Prof. Pedro A. Serena and Prof. Juan Jose Saenz. However, the TNT Conference series is the successful consequence of the effort of several organising Institutions (11 worldwide in 2005) that jointly organise and partially fund the TNT event.

TNT is now one of the premier European conferences devoted to nanoscale science and technology with around 400 participants, more than 60 speakers and 250 posters presentations.

One of the main objectives of the Trends in Nanotechnology conference is to provide a suitable platform where young researchers present their latest work, interacting with high-level scientists. For this purpose, the Organising Committee provides every year around 60 travel grants for students. In addition, more than 20 awards are given to the best contributions presented by young PhD students. More than 60 senior scientists are involved in the selection process. Grants and awards are funded by the TNT Organisation in collaboration with several institutions.

This high-level scientific meeting series aims, therefore, to present a broad range of current research in Nanoscience and Nanotechnology worldwide as well as related policies (European Commission, etc.) and initiatives (iNANO, IEEE, GDR-E, etc.). TNT events have demonstrated that they are particularly effective in transmitting information and establishing contacts among workers in this field. Graduate students fortunate to attend such events quickly learn the importance of interdisciplinary skills, thereby becoming more effective in their future research.

Invited Lectures

Harold Kroto (Florida State University, USA)
Heinrich Rohrer (Switzerland)

Keynote Lectures

Masakazu Aono (Nanomaterials Lab. NIMS, Japan)
Yoshio Bando (NIMS, Japan)
Jacques Beauvais (University of Sherbrooke, Canada)
Flemming Besenbacher (iNANO, Denmark)
Gerard Bidan (CEA-DRFMC, France)
Mei-Yin Chou (Georgia Tech, USA)
Russell Cowburn (Imperial College London, UK)
Oscar Custance (Osaka University, Japan)
Yves Dufrene (Universite Catholique de Louvain, Belgium)
Pedro Echenique (DIPC/UPV, Spain)
Jaime Ferrer (Universidad de Oviedo, Spain)
Peter Gruetter (McGill University, Canada)
Bret Heinrich (Simon Fraser University, Canada)
Peter Hinterdorfer (University of Linz, Austria)
Kikuji Hirose (Osaka University, Japan)
Maki Kwai (Tokyo University, Japan)
Colin Lambert (Lancaster University, UK)
Uzi Landman (Georgia Tech, USA)
Gustavo Luengo (L'OREAL Research, France)
Richard Martel (Montreal University, Canada)
Bill Milne (Cambridge University, UK)
Daniel Mueller (Technische Universitat Dresden, Germany)
Abraham Nitzan (Tel Aviv University, Israel)
Bibiana Onoa (Dupont, USA)
Pablo Ordejon (CSIC-ICMAB, Spain)
Yung-Woo Park (Seoul National University, Korea)
Michael Pustilnik (Georgia Tech, USA)
Eran Rabani (Tel Aviv University, Israel)
Ron Reifenberger (Purdue University, USA)
Siegmar Roth (M-P-I fuer Festkoerperforschung, Germany)
Miquel Salmeron (Lawrence Berkeley Laboratory, USA)
Ivan K. Schuller (UCSD, USA)
Clivia Sotomayor Torres (NMRC, Ireland)
Nongjian Tao (Arizona State University, USA)
Didier Tonneau (CRMCN/CNRS, France)
Kohei Uosaki (Hokkaido University, Japan)
Patrick Van Hove (EC-DG Information Society, Belgium)
Jose-Luis Vicent (Universidad Complutense de Madrid, Spain)
Robert A. Wolkow (University of Alberta, Canada)

Latest News About This Event At *http://www.tnt2005.org*

GDR on Science and Applications of Nanotubes (NanoE)

History

During the period 1998-2003, the French CNRS has promoted and financially supported the GDR 1752 ("Group of Research": official entity) focused on fostering national collaborations between researchers working in all the fields of carbon nanotubes. The activities were devoted to the organisation of annual meetings, thematic workshops, support of exchange visits between the teams belonging to the GDR, especially for training activities of PhD students. Starting in 1998 with 12 laboratories already active in the field, the group has evolved to include around 50 academic teams representing more than 250 researchers in 2003. In the same period, about 50 PhD theses were defended, more than 10 patents were deposited and about 300 publications were submitted, with 30% of joint papers involving several GDR members. A few industries were also involved such as Thales, Air Liquide, Motorola-France and Nanoledge.
The GDR has been successful in developing a large national research network, fostering collaboration and scientific advances. This has been achieved in particular thanks to the sharing, training and discussion aspects developed throughout the annual meetings, which have been very useful platforms of exchanges for initiating new collaborations, and for helping new people to be involved in the field, by being well informed about 'what is done and who is doing what'.

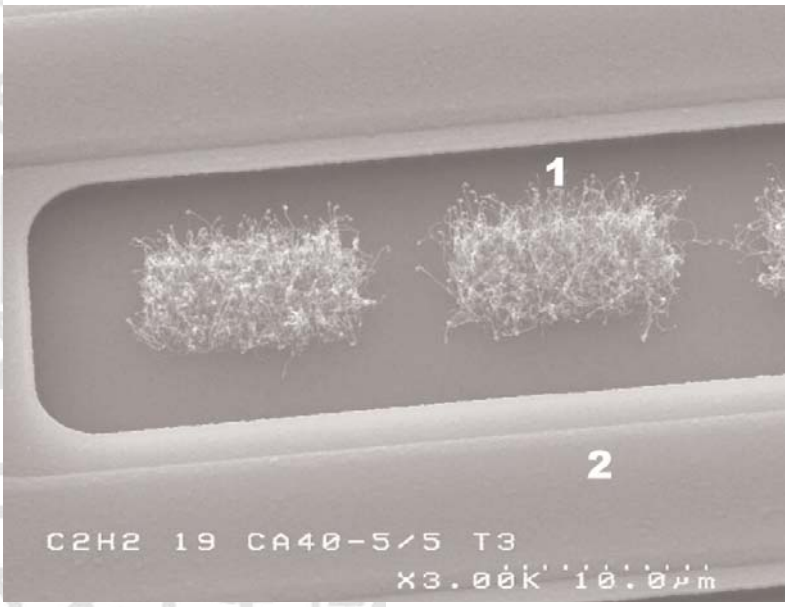


Figure 1:
SEM view of CNT integrated into the display structure.
The CNT are localized on catalyst pad, the pad dimensions are 5µm by 10µm.
The display pad density is $2.10^5 cm^{-2}$ There is few thousands of CNT for each pad
1-Pad with CNT / 2-Gate Electrode

GDR-E

On January 2004, this GDR was replaced by a European GDR (GDR-E) entitled 'Science and applications of the nanotubes' (acronym NanoE). This research group involves the French teams of the previous group and teams of different countries of the European Union. In France, this GDR is financially supported by the CNRS and the CEA, whereas the European teams receive support from their own organisms.

The scientific activities of the GDR-E group are focused on four primarily thematic objectives, under the guidance of specific coordinators.

To develop nanoelectronics made of nanotubes in order to fabricate passive or active electronic devices and components (thematic 1) - (Coordinator: Stephan Roche)
To control the chemical and/or electro-chemical funtionalisation of nanotubes in order to increase their dispersibility in liquids and reactivity (thematic 2) (Coordinator: Cecile Zakri)
To evaluate qualitatively and quantitatively the environmental impact of nanotubes and in particular their interaction with the molecules and organisms of the living world (thematic 3) (Coordinator: Sylvana Fiorito)
To increase our knowledge and understanding of the nanotube growth mechanisms for a better control of the structural characteristics of the nanotubes in order to develop production processes more optimized and adapted to the applications (thematic 4). (Coordinator: Nicole Grobert)

WEB site: http://www.cnrs-imn.fr/GDRE_NanoE/index.html

Thematic Priorities Description

Thematic 1: Nanoelectronics, Devices and Components
Coordinator: Stephan Roche (CEA/DRFMC)

1) Introduction
2) The realm of quantum physics
3) Towards new technologies
4) GDR-E Groups in Nanoelectronics
5) Image Gallery

1) Introduction

Carbon nanotubes are known to exist in two flavours, respectively metallic or semiconducting depending on their helical symmetry. Metallic tubes usually display exceptionally large mean free path and very low resistance close to the theoretical limit of the quantum resistance (h/e^2, h: Planck constant and e: electron charge). Semiconducting tubes show an energy gap downscaling with their diameter.

Chemical doping of semiconducting tubes has been demonstrated, as well as carbon tubes filling (with metals, fullerene molecules, etc), or surface functionalisation by grafting molecules with electrochemical techniques. Novel class of hybrid nanomaterials are thus available either to study quantum charge transport phenomena in complex heteroatomic mesoscopic systems, or to engineer novel functions to improve or complement the Silicon-based CMOS technologies.

The spectacular impact of the topology of atomic distribution on physical properties has been unprecedented in Condensed Matter Physics, and has triggered during the past 10 years a tremendous amount of scientific activities first and still with a more fundamental focus, addressing nanotubes intrinsic properties, and challenging electronic properties and universal concepts of quantum transport physics by using advanced characterization techniques (transmission and tunnelling microscopies, Raman studies, and mesoscopic transport measurements). In parallel, more applied research has progressively spread worldwide and carbon nanotubes are now becom-

ing a standard as nano-objects for bringing innovation in nano-electronics.

Since more than 10 years, European researchers have actively participated to bring excellence in carbon nanotubes Science and Technology, and current activities and results are clearly amongst the leading edge contributions to deepen understanding as well as to demonstrate the possibilities for innovative carbon nanotubes-based technologies.

2) The realm of quantum physics

Electronic properties of carbon nanotubes have been explored with a variety of experimental techniques, over a wide range of temperature, by using magnetic fields and depending on contact geometry and materials.

The specificity of carbon nanotubes physics comes first from their **reduced dimensionality**, since diameters range from 1nm to few tens of nanometers, while nanotube length can be upscaled up to several microns or more. Physics in quasi-one dimensional systems is known to become more complex in regards to conventional materials for plenty of reasons. First, the contribution of electronic confinement, localisation phenomena, electron-phonon or electron-electron interaction due to the reduction of screening effects is enhanced. This makes the description of intrinsic transport at the same time more complex but also challenging since carbon nanotubes on the other side offer relatively simple systems for realistic modelling of both real space orbitals distribution and consequent electronic spectra.
For instance, it is possible to challenge the joint contribution of bandstructure effects and quantum interference effects in multiwalled nanotubes, or to investigate on the possibility to unveil signatures of non-Fermi liquid (such as Luttinger Liquid) by analysing current-voltage abnormalities beyond the linear response. *(See http://www.cnrs-imn.fr/GDRE_NanoE/ABachtold.htm)*

Figure 2
Carbon Nanotubes-based Field Emission Display (6 inches) from CEA/LETI technologies (courtesy of Jean Dijon)
The display definition is 320*240 with a brightness of 500Cd/m2
The pixel size is 350µm

Notwithstanding, an important observation is the fact that one can not easily elaborate on some universal framework for carbon nanotubes physical properties, since single-wall nanotubes, multiwalled or hybrid nanotubes will manifest different signatures due to severe **change of transport dimensionality**, **specific resonances, conductance patterns and different interfacing properties with contact materials**.

The second specificity when exploring nanotube electronics is **the contact issue.** Indeed, depending on nanotube geometrical features (for instance band-gap value of semiconducting tubes), and the nature of metallic contacts (Pd, Ti, Au,..) and contact geometry, the resulting charge injection properties at nanotube/metal interfaces will be very different. For metallic nanotubes, the contact nature ranges from ohmic and transparent contacts with little backscattering, to highly resistive contacts dominating electrical response as a consequence of interface quality and orbital bonding phenomenon. Contacting semiconducting nanotubes with metals also yield the possibility to get Schottky contacts that will dominate the transport physics of the nanotube-based field effect transistor. *(See http://www.cnrs-imn.fr/GDRE_NanoE/VDerycke.htm)*

All this demands to explore electronic phenomena in carbon nanotubes-based systems and devices with care, and to dedicate effort for showing how some particular physical properties suffer from upscaling either the tube diameter, the number of walls constituting the nanotube, or by changing the nature of contact material, and other environmental circumstances.
The understanding of fundamental concepts in carbon nanotubes transport definitely needs for theoretical modelling and advanced quantum simulation. Theory has been very important to initiate, validate and orientate carbon nanotube Science, particularly as far as electronic properties are concerned. Yet, in 1992 one year after Nanotube discovery by Prof. Sumio Iijima, several groups theoretically predict their unique behaviour as metals or semiconductors. To explore in details nanotube electronic or vibrational spectra, theory has been essential. The investigation of transport physics is also clearly demanding for advanced experimental studies sustained by theoretical support.

3) Towards new technologies

Proofs of concepts have been reported in several fields of technologies using nanotubes as field emission tip, or ballistic field-effect transistors (CNT-FETs).

Indeed, CNT-FET technologies that show promising perspectives since, at the level of the single device, such novel device outperform their Silicon-based counterparts in many aspects. However, CNT-based nanoelectronics with an extensive use of CNT-FETs is still beyond the scope of industrial developments, and much coordinate research efforts are still to be developed to make the CNT-technology mature enough to become mainstream technology.

The story of carbon nanotube based technologies is however just in the starting blocks. Much effort, coordination and cooperation is needed to make carbon nanotube a new standard materials for nanoelectronics, either for replacing metals in interconnects, or to engineer nanotube-based field effect transistors that will be highly performant, easily integrable into conventional CMOS technologies in a first stage, and with the possibility, only offered by a control chemically synthesis, to massively integrate nanotubes devices on large scale wafers.

European industrials have already started to consider nanotubes as a novel innovation for nanoelectronics. For instance, the German company INFINEON has reported on several breakthroughs in designing nanotube-based devices by using CVD growth, and French CEA has launched a new programme to foster the development of nanotube-based technologies.

Fig.2 shows the first European demonstration of CNT-based field emission display that result from a CVD growth assembly of multiwalled carbon nanotubes. This 6-inches panel is a result of advanced research developments performed in CEA/LETI, research programme that also benefited from European research network launched during the fifth framework of European Commission programme.

4) GDR-E Groups in nanotube (Nano)-electronics

The following list is to establish the members of GDR-E that have some research activities in relation with experimental or theoretical characterisation of electronic properties of carbon nanotubes in the broad sense. The groups here have demonstrated important contributions to the field, either by investigating electronic properties of tubes with advanced spectroscopic methods, transport or AFM/STM measurements.

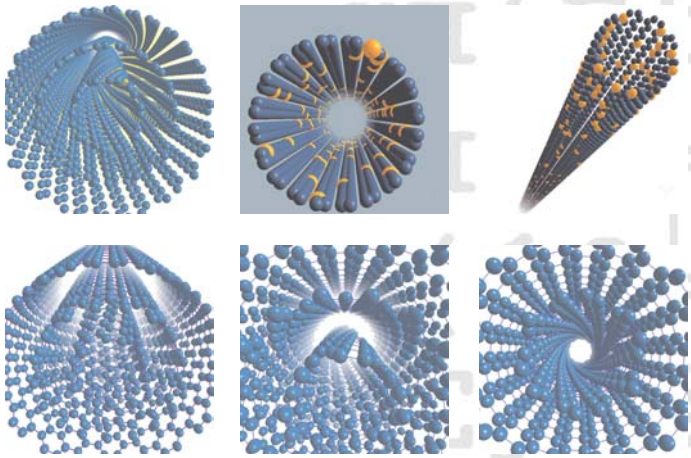
Theoretical groups

Xavier Blase (Lyon)
Jean-Christophe Charlier (Louvain La Neuve)
Michel Devel (Besancon Univ.)
François Ducastelle (ONERA Paris)
Jean-Pierre Gaspard (Liege Univ.)
Malcom Heggie (Sussex Univ.)
Philippe Lambin (Namur Univ.)
Stephan Roche (CEA/DRFMC Grenoble)
Angel Rubio (DIPC San Sebastian)

Electronic and Transport Physics experimental groups

Adrian Bachtold (ENS Paris and CSIC Barcelona)
Hélène Bouchiat (ORSAY, LPS)
Vincent Bouchiat (CNRS, Grenoble)
Jean-Philippe Bourgoin (CEA, Saclay)
Jean Dijon (CEA/LETI, Grenoble)
Julio Gomez (UAM, Madrid)
Serge Lefrant (INM, Nantes)
Ahmed-A Zahab and Philippe Poncharal (Montpellier Univ.)
Steven Purcell (Claude Bernard-Lyon)
Jean-Marc Broto and Bertrand Raquet (LNCMP, Toulouse)
Jean-Paul Salvetat (Orleans)
Jean-Louis Sauvajol (Montpellier Univ.)
Christoph Strunk (Regensburg Univ)
Jean-Eric Wegrove (Polytechnique Palaiseau)

5) *Image Gallery (by Stephan Roche)*



Thematic 2: Chemical functionalization and dispersability of nanotubes

Coordinator: Cecile Zakri (CRPP Bordeaux)

Introduction

One of the major hindrances in the use of nanotubes for a lot of applications is their manipulation. Chemistry allows one to chemically or electro-chemically 'manipulate' the nanotubes. One aspect of this manipulation consists in separating them as a function of their diameter and/or their helicity, or in purifying them (removing impurities from the pristine powder). Another important aspect is to make them compatible with different media (liquids or solids) into which they are to be inserted (composites), to elaborate hybrid nanomaterials having well-defined functionalities (ultra sensitive chemical or bio sensors), or to use the nanotube as a tool (support for synthesis).

The contribution of chemistry to nanotube science and applications

Manipulations can for example consist in grafting selected molecules on their surface, inserting objects in their central cavity or fabricating micelles or colloidal systems. The future of several types of applications depends on the control of functionalisation. This is one of the major preoccupations of this domain. Because this research in France is rather underdeveloped, one of the objectives of the GDR-E will be to mobilise and to structure different expertises. The Aussois school has already permitted to engage an extensive thinking on these questions with a number of specialists ready to invest themselves and to explore new paths such as electrochemistry. The European structure of the new GDR is also a real asset to connect the different teams working in this domain. Recent works on grafting, on utilizing surfactants or colloids should serve as inspiration for this line of the GDR-E. One notes that most of the groups have already been involved in European structures (TMR network FUNCARS "Functionalisation of Carbon Nanotubes" which ended in April 2003) for which the guiding principle was to train a whole new generation of researchers in these new concepts.

Different aspect of the thematics	Possible Applications (Non Exhaustive)
Dispersion and Purification of nanotubes	Processing, Sorting, etc.
Functionalisation of Nanotubes	Sensors, Biosensors, Support for Synthesis
Insertion of Nanotubes	Mechanical Reinforcement, Electrical or Thermal Components
Electrochemistry of Nanotubes	Sensors, Electrodes, Actuators, Super-Capacitors
Doping or Filling of Nanotubes	Electronics, Containment, Storage

Organisation and contact details

GDR-E is driven by Annick Loiseau, assisted by Jean-Louis Sauvajol, Philippe Lambin and Patrick Bernier.

More information: http://www.cnrs-imn.fr/GDRE_NanoE/Organ.htm

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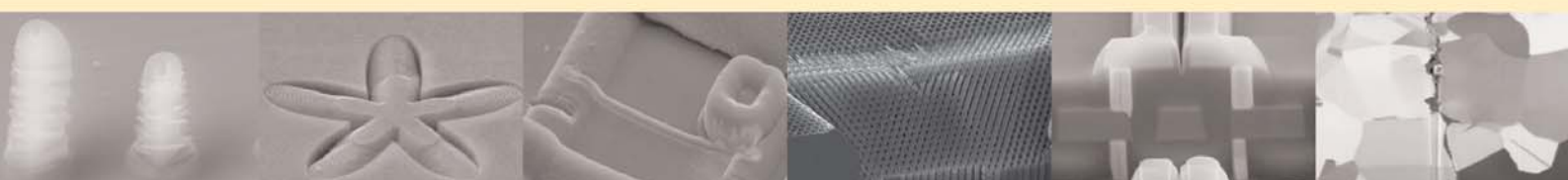

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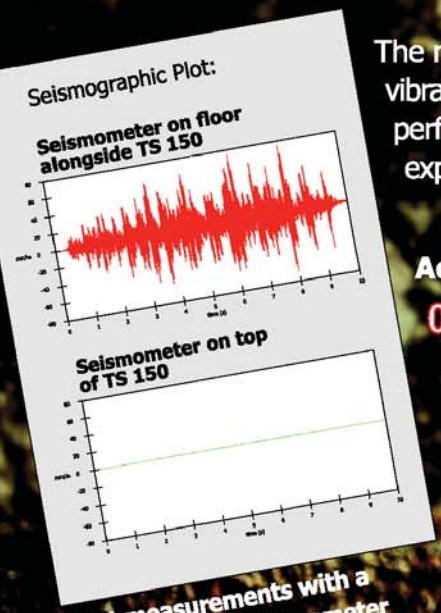

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