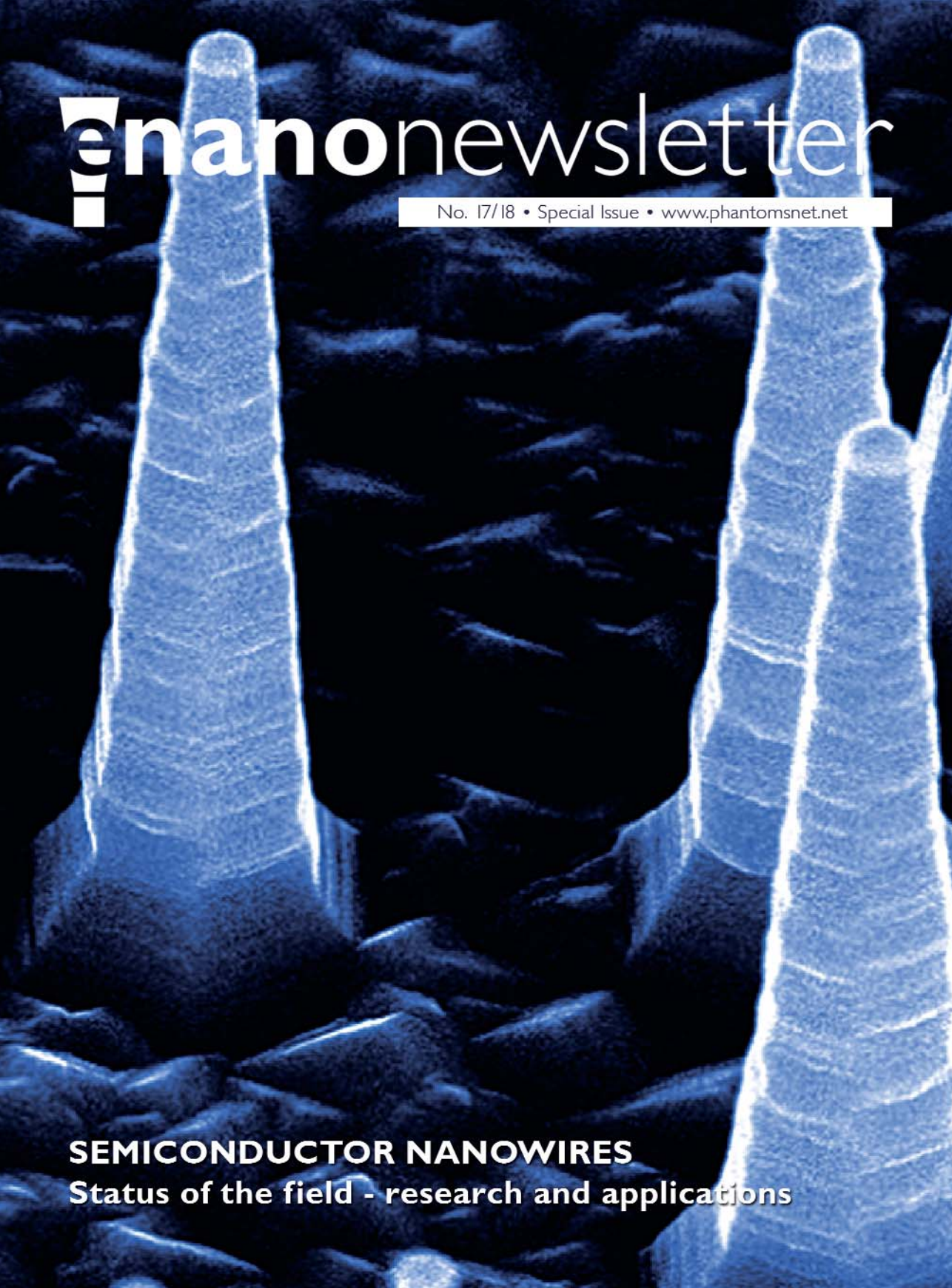

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SEMICONDUCTOR NANOWIRES

Status of the field - research and applications

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Dear Readers,

This E-nano Newsletter special double issue contains a report providing insights in a relevant field for nanoscale devices research that has developed very rapidly during the last five years: semiconductor nanowires (NW).

Nanowire-based devices offer unique opportunities in different research areas and represent a possible impact as key add-on technologies to standard semiconductor fabrication.

The nanoICT position paper provides an analysis of the current status of nanowires research and applications at the nanoscale in several areas of interest: nanowire-based electronics, fundamental studies of nanowire growth, opportunities for opto-electronic devices based on NW technology, application for Energy harvesting as implemented in solar cells and thermoelectrics and finally their use in biology and in medical applications.

We would like to thank all the authors who contributed to this issue as well as the European Commission for the financial support (project nanoICT No. 216165).

Dr. Antonio Correia
Editor - Phantoms Foundation

Deadline for manuscript submission
Issue No. 19: June 30, 2010
Issue No. 20: August 31, 2010

Depósito legal/Legal Deposit:
M-43078-2005

Impresión/Printing:
Madripapel, S.A.

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Semiconductor nanowires: Status of the field - research and applications

Editorial Information

No. 17/18
December 2009
March 2010
Published by Phantoms Foundation (Spain)

1500 copies of this issue have been printed.
Full color newsletter available at:
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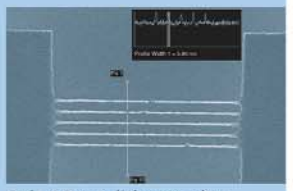

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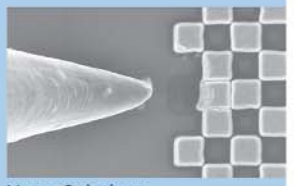

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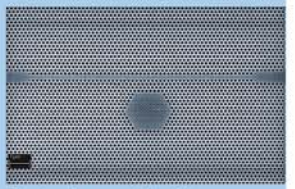
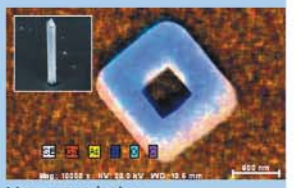


Photonic crystal with proximity effect correction



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Semiconductor nanowires: Status of the field - research and applications

Introduction

List of experts / Contributors: With the core of this report based on the final publishable report from the EU/IST funded NODE-project, basically all 12 partners of this program have contributed in different ways. Most significant have been the over-all coordination by C. Thelander and L. Samuelson (Lund University) and the site leaders of the 12 partners: L-F. Feiner (Philips), W. Riess (IBM), G. Curatola (NXP), L. Ledebo (QuMat), W. Weber (NamLab, previously Qimonda), J. Eymery (CEA), U. Gösele (MPI), P. Vereecken (IMEC), L. P. Kouwenhoven (TU Delft), A. Forchel (Univ. Würzburg), A. Tredicucci (SNS-Pisa). Other people that have contributed are V. Zwiller (TU Delft), J-C Harmand and P. Caroff (LPN-CNRS), J. Johansson, C. Prinz, J. Tegenfeldt, K. Deppert and H. Linke (Lund Univ.). Many others have directly and indirectly contributed to this report.

Keywords: Nanowire, growth, processing, physics, characterization, devices, integration, energy, biology.

Institutions acronyms:
LU: Lund University; **PRE:** Philips Research Laboratory Eindhoven; **MPI:** Max-Planck-Institut; **IBM:** IBM Zurich; **WV:** University Wurzburg; **QM:** QuMat; **TUD:** Technical University of Delft; **NL:** NamLab, previously Qimonda; **IMEC:** Interuniversity Microelectronics Center; **SNS:** Scuola Normale Superiore di Pisa; **CEA:** Commissariat à l´Énergie Atomique; **CNRS/IEMS:** Centre National de la Recherche Cientifique / Institut d´Electronique, de Microelectronique et de Nanotechnologie.

The field of semiconductor nanowires (NWs) has during the last five years developed very rapidly. Within the European frame-work the strongest efforts have been in the development of nanowire-based electronics, i.e. nanowire transistors, as performed in the largest Integrated Project within "Emerging Nanoelectronics", called "Nanowire-based One-Dimensional Electronics (NODE)". Considering the rather high maturity of the research field reached through NODE, we use the final publishable report as the core of this report. We also attach as an appendix a summary of impressions from the dissemination workshop that was organized at the conclusion of NODE, when the "NODE Workshop on Nanowire Electronics" was organized in Lund in September 2009. Here we also summarize the input and recommendations as provided by the invited experts: W. Hänsch (IBM), M. Passlack (TSMC), J. Knoch (TU Dortmund), T. Mikolajick (NAMLAB), H. de Man (IMEC), and L. Tilly (Ericsson).

Other central areas of nanowire research and applications deal with fundamental studies of nanowire growth, as very actively pursued through the arrangements of a series of four European Workshops on Growth on Nanowires, most recently the 4th arranged in Paris in October 2009. We include as an appendix a summary of the status as revealed from this workshop (written by J-C Harmand and F. Glas). Incorporated in this article is also a status of the field description provided by J. Johansson and P. Caroff.

In order to provide a more detailed description of the level of understanding and control of physical properties of nanowires, a special chapter has been provided for this by L. P. Kouwenhoven and V. Zwiller. This chapter also deals in more detail with the opportunities for opto-electronic devices based on NW technology.

Another important area of NW research relates to their application for Energy harvesting as implemented in solar cells and thermoelectrics. For the use of NWs in photovoltaics was recently started an EU-project called AMON-RA. We enclose two short descriptions of Nanowires for energy, provided by K. Deppert.

An increasingly important aspect of nanowire research deals with their use in biology and in medical applications. We include here also a description of the state of the art as provided by C. Prinz and J. Tegenfeldt. For each of these areas we try to provide some of the key references but these are far from complete lists of references.

1. Overview of nanowire electronics[1]

The integrated project "NODE" developed and evaluated technologies for growth and processing of semiconductor nanowire devices for their possible impact as key add-on technologies to standard semiconductor fabrication. The partners in NODE worked on generating a deepened understanding of the physics phenomena of one-dimensional semiconductor materials and nanowire-based devices, and on developing new functionalities not found in traditional higher-dimensional device structures.

[1] Based on the NODE project executive summary

A set of key device families based on semiconductor nanowires were studied in detail; such as tunneling devices, and field-effect transistors. Also unique opportunities that may be offered by nanowires in different areas are explored, e.g. memory applications. NODE maked a dedicated effort to evaluate the potential for integration of nanowire-specific processing methods and to assess the compatibility with requirements from conventional semiconductor processing, as well as evaluating novel architectural device concepts and their implementation scenarios. This chapter is based on the NODE project executive summary. Detailed information about objectives and main achievements of the NODE project are available in Annex 2.

I.I. Nanowire growth

I.I.I. General growth control

Controlling the crystal structure of InAs nanowires (LU)

Gold-particle seeded nanowires fabricated in materials with zinc blende as the bulk crystal structure are often observed to have wurtzite crystal structure. The general trend is that thin wires are wurtzite and thick wires are zinc blende. That is, there is a cross-over diameter for the preferential polytype. This cross-over diameter is temperature dependent. By carefully varying the temperature during growth we were able to fabricate superlattices with alternating zinc blende and wurtzite structure. [1]

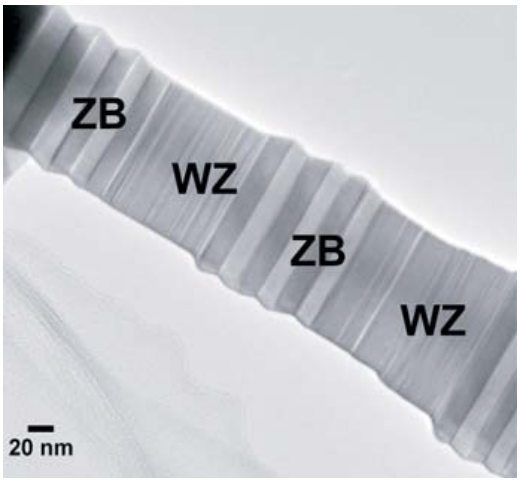

Fig 1. Polytypic superlattice, with alternating zinc blende and wurtzite structure, along an InAs nanowire.

Crystal phase and twin superlattices (PRE)

The crystal phase of III-Vs NWs can be determined by the dopant precursor flows during growth. In InP the use of Zn-precursor favors the ZB phase, whereas the use of S-precursor favors the Wz phase. Moreover, highly regular twin superlattices can be induced in the ZB phase by tuning the Zn concentration, wire diameter and supersaturation. The effect was explained in a model based on surface energy arguments. [2]

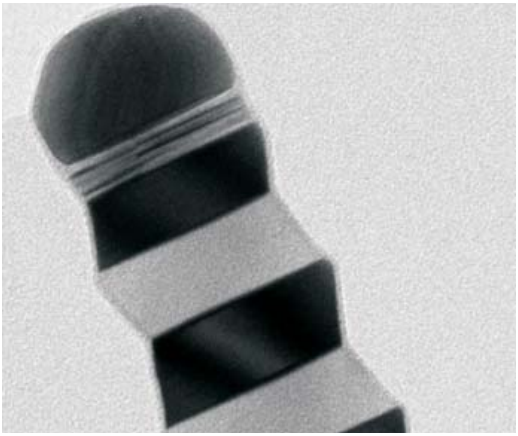

Fig 2. TEM image of the top part of an InP NW, closely below the Au catalyst particle, showing the highly regular twin superlattice structure.

Synergetic growth (PRE)

A counter-intuitive effect controlling the influence of wire spacing on growth rate was uncovered, synergetic

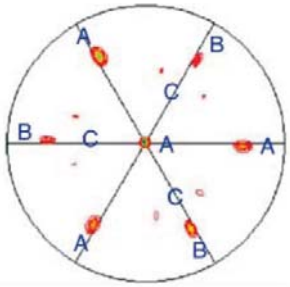

Fig 3. GaP wires next to a thick wire are taller than the second-nearest wires, which are taller than those in the middle of the field (furthest from the thick wire), showing that the growth rate of one wire is enhanced by the presence of another one and dependent on the catalytic alloy amount.

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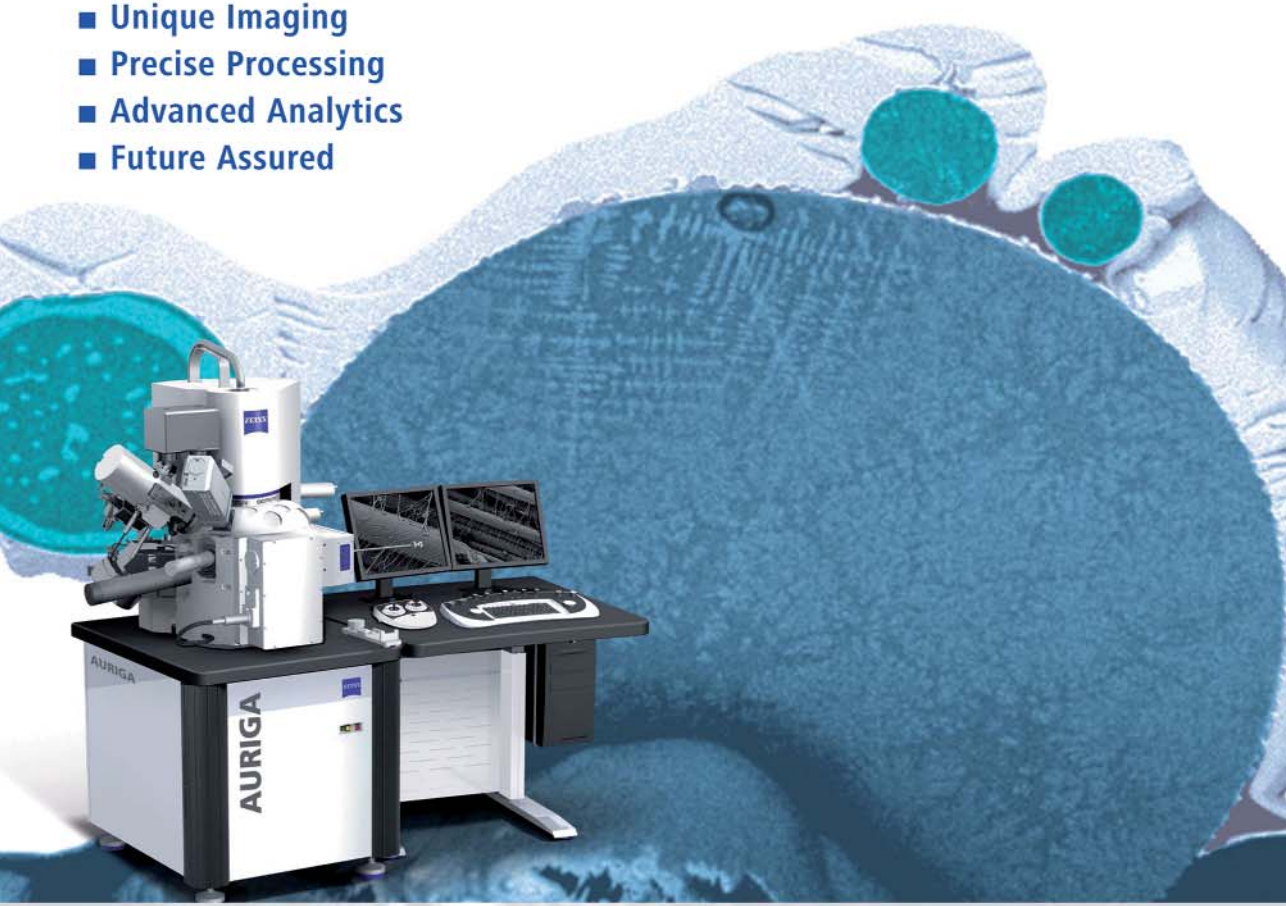

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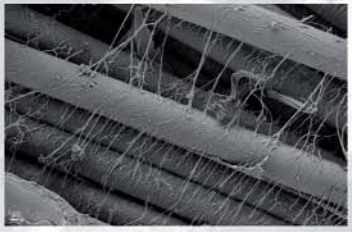
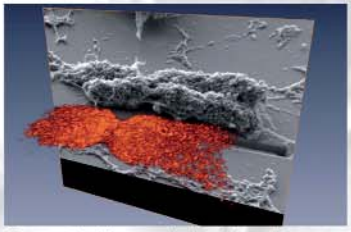
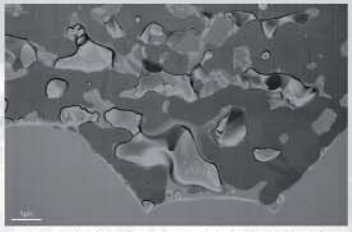


Chamber SE image of an uncoated fibre adhesive (used in modern shipbuilding). Taken with local charge compensation at 5 kV.



3D reconstruction of chromosomes based on real-time movie. Taken with in-lens SE detector at 2 kV. Courtesy of Prof. G. Wanner, Munich, Germany.



Cross section through the front contact of a Si wafer-based solar cell. Taken with in-lens SE detector at 2 kV. Courtesy of Dr. F. Machalett, ersol Solar Energy AG, Erfurt, Germany.

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growth, which implies that at smaller spacing the competition for available material, reducing the growth rate, is counteracted by the increase in surface density of catalyst metal particles on neighboring nanowires, providing more decomposed material. [3]

I.I.2. Heterostructures

Epitaxial Ge/Si nanowires (MPI)
Epitaxial Ge/Si hetero-structure nanowires on Si (100) substrates were prepared in AAO templates. Usually, the Si atoms dissolved in the Au/Si eutectic catalyst act as a reservoir for Si, and the interface to Ge is smeared out. This new approach of the growth inside the AAO templates, allowed to produce a sharp interface of Ge/Si without changing the diameter of the nanowire. [4]

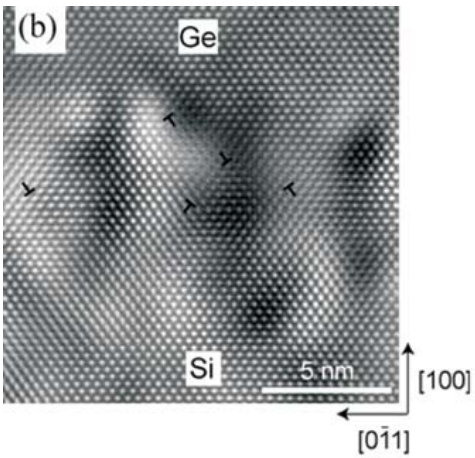

Fig 4. Cross-section TEM ima-ge of the Ge-Si interface.

Morphology of axial heterostructures (LU)
An extensive investigation of the epitaxial growth of Au-assisted axial heterostructure nanowires composed of group IV and III–V materials have been carried out and derived a model to explain the overall morphology of such wires. [5]

By analogy with 2D epitaxial growth, this model relates the wire morphology (i.e., whether it is kinked or straight) to the relationship of the interface energies between the two materials and the particle. This model suggests that, for any pair of materials, it should be easier to form a straight wire with one interface direction than the other, and this was demonstrated for the material combinations presented here.

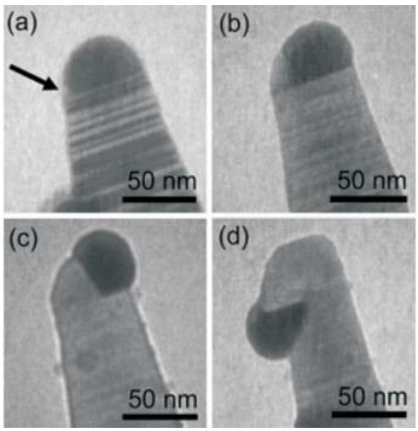

Fig 5. Images recorded during the growth of Ge on GaP nanowires by UHV-CVD.

I.I.3. Doping

Decoupling the radial from the axial growth rate by in situ etching (LU)
It was shown that in-situ etching can be used to decouple the axial from the radial nanowire growth mechanism, independent of other growth parameters. Thereby a wide range of growth parameters can be explored to improve the nanowire properties without concern of tapering or excess structural defects formed during radial growth. We used HCl as the etching agent during InP nanowire growth, and etched nanowires show improved crystal quality as compared to non etched and tapered NWs. These results will make way for devices relying on doping in axial structures, where any radial overgrowth would lead to short circuiting of a device.

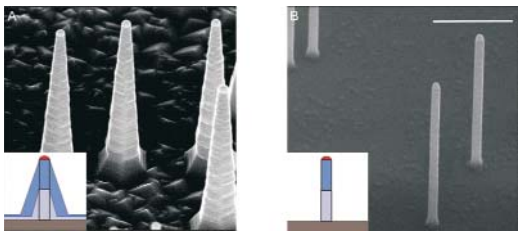

Fig 6. a) Tapered reference InP nanowires grown at a temperature of 450ºC, b) Non tapered nanowires grown with HCl in the gas phase under otherwise identical growth conditions to a).

P-type doping and p-n junctions in InP NWs (PRE)

Sulphur was identified as a suitable candidate for n-type doping of InP in MOVPE using H_2S as a precursor. It was

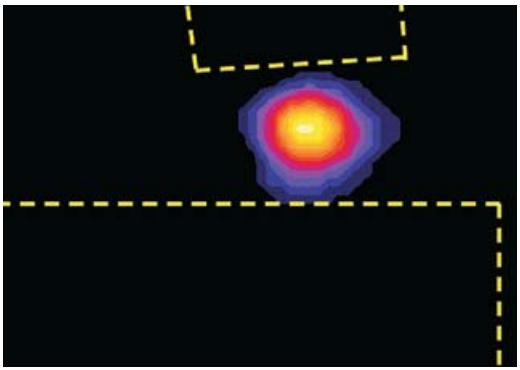

Fig 7. Optical microscope image of electroluminescent light coming from an InP NW LED, as collected by a CCD camera (the dashed lines show the positions of the electrodes).

further established that Zn-doping can be effectively used to achieve p-type doping in InP, using trimethylzinc as a precursor. The combination of S and Zn permits realization of p-n junctions in InP, showing good electrical diode characteristics in thin (20 nm-diameter) nanowires. The diodes exhibit LED behavior, testifying the high quality of the p-n junctions. [6]

Remote p-type doping of InAs NWs (PRE)

Obtaining quantitative control of doping levels in nanowires grown by the vapor-liquid-solid (VLS) mechanism is

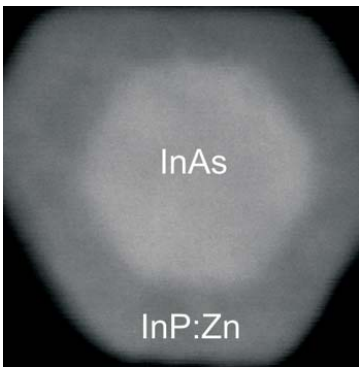

Fig 8. Dark-field TEM image of the InAs(core)/InP:Zn(shell) NW.

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especially challenging for the case of p-type doping of InAs wires because of the Fermi level pinning around 0.1 eV above the conduction band. It was shown that growing a Zn-doped shell of InP epitaxially on a core InAs NW yields remote p-type doping: shielding with a p-doped InP shell compensates for the built-in potential and donates free holes to the InAs core. The effect of shielding critically depends on the thickness of the InP capping layer and the dopant concentration in the shell. [7]

1.1.4. Si integration

Al as catalyst for Si nanowires (MPI)
Replacement of Au by other catalysts was one of the main efforts of this work. The metal Al was successfully used as a catalyst at low growth temperature in the VSS mode for growth of freestanding Si nanowires. The template-assisted growth using AAO and Al catalyst allowed to grow (100) oriented Si nanowires. [8]

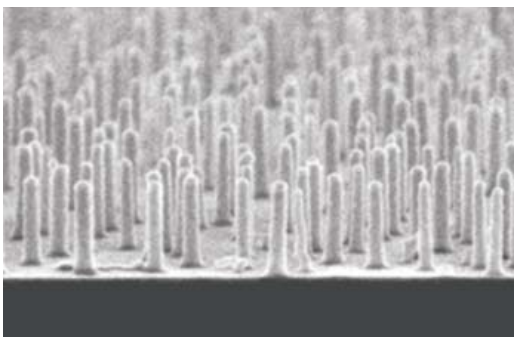

Fig 9. Si nanowires grown by use of a Al catalyst.

Epitaxial growth of III-V NWs on Si and Ge (PRE)
The growth of GaAs, GaP, InAs, and InP nanowires on Si and Ge substrates was investigated extensively , and high-quality epitaxial growth was demonstrated for these materials systems. It was shown that the orientation of the epitaxial nanowires depends on the substrate-wire lattice mismatch. [9]

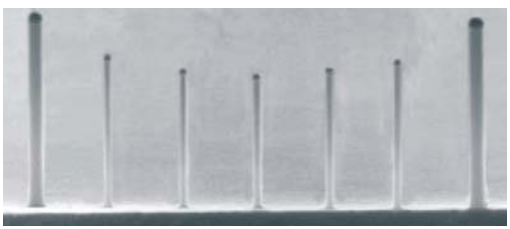

Fig10. X-ray diffraction pole measurements on InP wires grown on Si(111), showing the presence of InP(111) reflections originating from the wires.

Au-free InAs nanowires on silicon (LU)
Narrow bandgap materials, such as InAs, could have great impact on future nano-electronics if integrated with Si, but integration has so far been hard to realize. InAs nanowires can be grown directly on silicon substrates using a method employing self-assembled organic coatings to create oxide-based growth templates. [10] The method was subsequently modified to also allow for position-control, which is required for vertical device implementation.

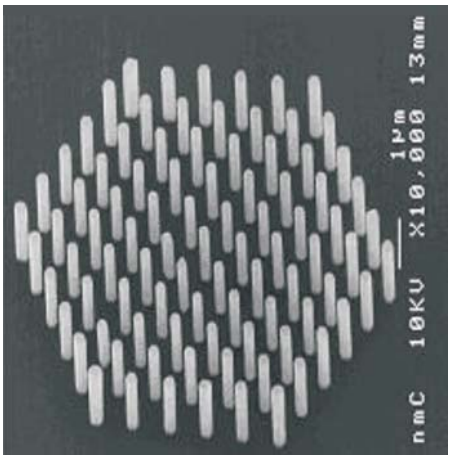

Fig 11. Epitaxial InAs nanowires grown on a Si(111) substrate from holes etched in a SiO_2 film.

1.2. Nanoprocessing

1.2.1. Surface passivation and gate dielectrics

Lateral nanowire n-MOSFETs (IBM)
Fully depleted lateral n-channel MOSFET devices were fabricated using implantation for source and drain regions. Strong inversion and clear saturation currents are observed in FETs from intrinsic NWs with p-implanted source/drain regions, whereas NWFETs with Schottky contacts only operate in accumulation mode.

The effect of surface preparation on the electrical characteristics were studied and revealed that encapsulating the devices in a protective oxide yields significantly increased on currents and steeper sub-threshold swings. [11] This analysis reveals the strong influence of the electrostatics on the transport properties and shows that the extraction of device parameters using conventional models may not be valid.

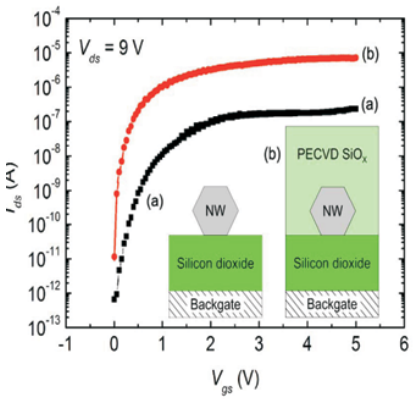

Fig 12. Transfer characteristic of a lateral nanowire n-MOSFET as fabricated surrounded by air (black) and encapsulated in SiO_2.

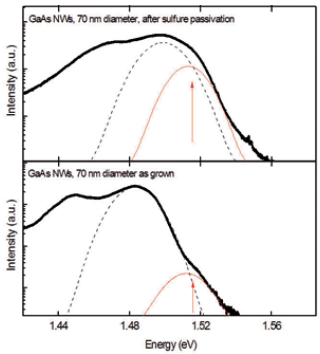

Fig 13. Photoluminescence spectrum of an as grown (bottom) and a passivated wire (top).

Chemical passivation of nanowires (WU)

The large surface to volume ratio of nanowires makes them very sensitive to surface effects such as nonradiative recombination centers or trapped charges. Surface passivation of GaAs nanowires by difference chemical treatments has been investigated and an improvement of the luminescence efficiency by a factor of 40 compared to as-grown wires could be achieved.

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1.2.2. Contacts and gates for nanowire FETs

50 nm L_g Wrap Gate InAs MOSFET (QM)

Wrap Gated, or gate all around devices show the best control of the channel potential. InAs high-κ (HfO_2) oxide nanowire field effect transistor, were successfully fabricated with a 50 nm long wrap gate. The first transistors were based on InAs wires grown on a n+ InAs substrate. The high mobility and injection velocity of the InAs channel leads to a good drive current and excellent transconductance. [12]

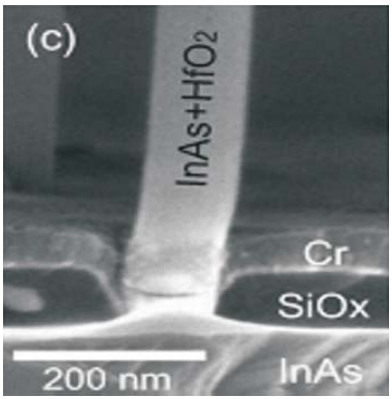

Fig 14. Cross section of the MOSFET, showing the 50 nm Cr gate around the InAs nanowire.

Schottky barrier FETs (IBM)

The use of thin Si_3N_4 interface layers between the silicon and metal contacts were shown to give Ohmic contacts whereas without the Si_3N_4 a normal Schottky contact was achieved. Furthermore, it was demonstrated that the Si_3N_4 interface layer gives Schottky barrier FETs with suppressed ambipolar behaviour due to a reduction in metal induced gap states. [13]

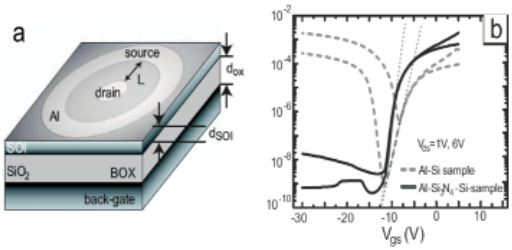

Fig 15. Schematic of a Schottky barrier pseudo-MOSFET and the corresponding transfer characteristics with and without an interface layer.

Multiple gates for nanowire devices (TUD)

Nanowires with multiple gates on horizontal nanowires have been developed to create electrical quantum dots in InAs/ InP nanowires. These devices are used to investigate quantum effects in coupled quantum dots nanowires. [14]

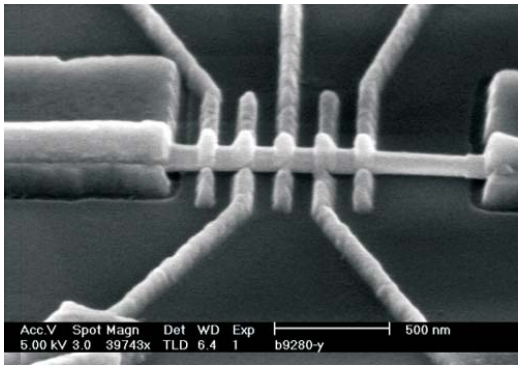

Fig 16. Horizontal InAs/InP nanowire with multiple gates.

Nanowire FET with gated Schottky contact (WU, NL)

Gated Schottky contacts allow a control over the polarity of the injected carriers, allowing to switch the operation of a nanowire FET from n-type to p-type. Such devices can be used to realize complementary logic without doping the nanowires.

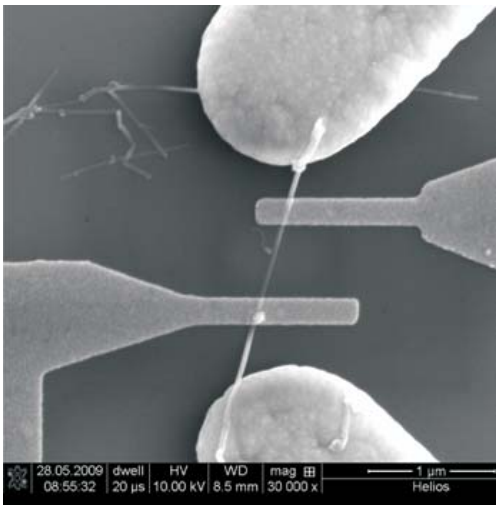

Fig 17. Si-nanowire FET with two gated Schottky contacts.

Wrap-around gate vertical Si nanowire Tunnel-FETs (IMEC)

The NODE project successfully developed a CMOS compatible process flow to fabricate vertical Si nanowire Tunnel-FETs using state-of-the-art processing tools onto 200mm wafers. An advanced gate stack using high-κ (HfO_2) oxide and metal gate (TiN) was implemented.

The top contact was obtained by isotropic dry etch of the gate stack at the top of the wire using a gate hard-mask. The gate is isolated from the substrate by a thick oxide layer. It is also isolated from the top contact by a nitride spacer and oxide layer. A capping layer connects multiple wires together. Top contact doping is achieved through epitaxial layer or tilted implants.

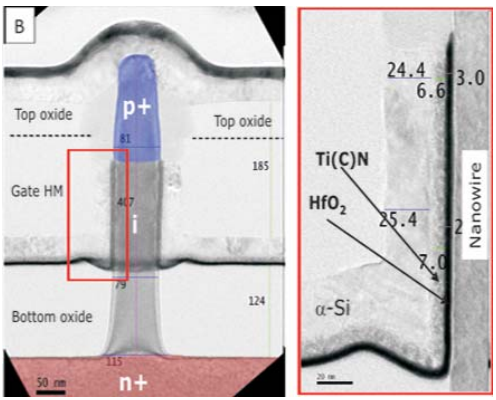

Fig 18. Cross section of the vertical TFET featuring 3nm HfO_2, 7nm TiN and 25nm a-Si gate stack around the nanowires.

1.2.3. Processing of vertical nanowire devices

InAs Wrap Gated MOSFETs for RF and circuit applications (QM/LU)

For RF and circuit applications, the transistors need to be integrated on an highly resistive, or insulating substrate. Technology for growing, and locally contacting InAs nanowires on a semi insulating InP substrate has been developed.

The technology is based on a local ohmic substrate contact, which wraps around the base of the nanowires. This allows for RF characterization of the InAs MOSFETs, with first results of f_t=7 GHz and f_{max}=22 GHz. [15]

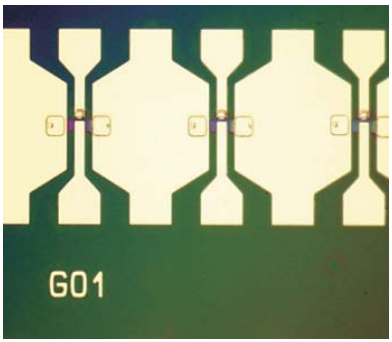

Fig 19. Top view of a fully processed RF-compatible vertical nanowire transistor structure.

Vertical Impact Ionization MOS FETs (IBM-ZRL)

A process for vertical silicon nanowire FETs was developed. Using this process vertical impact ionization FETs with sub-threshold swings down to 5 mV/dec. were demonstrated. [16]

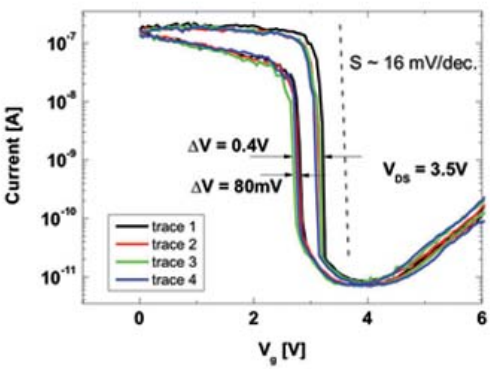

Fig 20. Stability of the transfer characteristics of a vertical IMOS FET.

Nanowires based spin memory (TUD)

The NODE project created a spin memory in a single quantum dot embedded in an InP nanowire. The preparation of a given spin state by tuning excitation polarization or excitation energy demonstrated the potential of this system to form a quantum interface between photons and electrons.

For this purpose, transparent contacts on vertical nanowires have been developed for FET devices and are currently under investigation. [17]

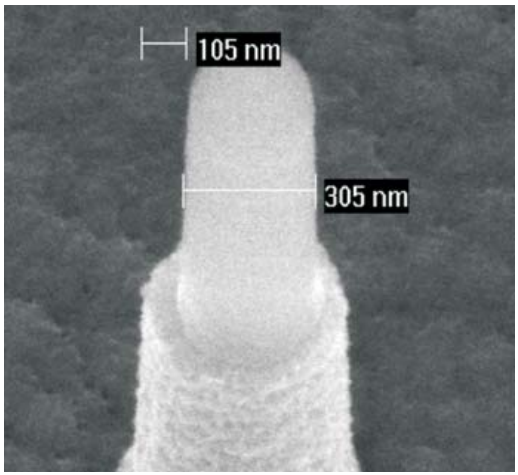

Fig 21. Vertical nanowire surrounded by a dielectric and a wrap gate.

SiO_2 template development for catalyst-free nanowire growth (IMEC)

A process was developed to fabricate hole patterns on top of silicon for constrained growth of Si nanowires, without the use of catalyst. The template was prepared by patterning a plasma–enhanced chemical-vapor deposited (PE CVD) Si_3N_4/SiO_2 25nm/300nm film stack

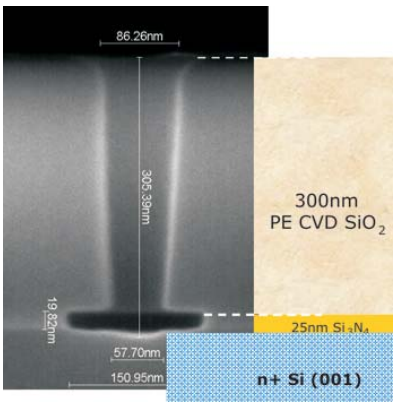

Fig 22. Cross-section of a via hole after plasma etch and hot phosphor opening of the Si_3N_4 bottom layer.

with openings or holes to expose the underlying Si. The patterning was performed through 193nm lithography and etching of the SiO_2 with Motif®, an advanced dry etch technique capable of shrinking printed feature sizes thanks to the deposition of a polymeric coating on top of the developed resist. Particular care was dedicated to cleaning of the side walls and the silicon bottom substrate to avoid defects creation during subsequent growth. To achieve suitable Si purity for epitaxial growth, a special sequence of process steps was needed to avoid Si contamination by carbon residues from etch.

1.3. Physics and characterization

1.3.1. Electrical properties

Room temperature transport (SNS)

Room temperature transport properties of bare InAs and InAs/InP core shell nanowires [18] have been studied and a three dimensional electrostatic model was developed to compute the NW FET capacitance for a more accurate mobility determination. The measured values ranged in the 1-2 thousand cm^2/Vs for the thinnest wires (< 40 nm), while reached about 3 thousand for thicker wires. Remarkably all the wires showed relatively low values of electronic charge in the few $10^{16}cm^{-3}$ range. The highly Se-doped wires revealed an attendant strong increase in charge density up to ~ $1x10^{19}cm^{-3}$; as expected the impurities introduced brought along a decrease in the mobility, which varied in the 4-6 hundred cm^2/Vs range for wire diameters of 40-50 nm. In parallel, NW devices were fabricated for charge pumping through surface acoustic waves (SAW) [19]. The NW FETs were implemented on top a $LiNbO_3$ substrate with piezoelectric transducers. An acoustoelectric current peak in the wire was identified when driving the transducer near its resonance frequency. This type of devices is quite interesting both for analog signal processing and for the implementation of single-photon sources under quantized charge pumping.

Furthermore, it yields a new direct method to measure the carrier mobility by observing the bias point at which the acoustoelectric peak in the current changes of sign, signaling that drift and acoustic wave velocity are the same.

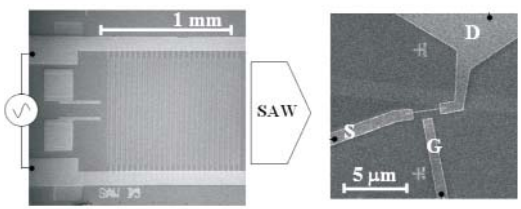

Fig 23. Sketch of the device and set-up for the induction of acoustoelectric current in NW FETs.

Diameter dependence of tapered InAs nanowires [20] (TUD, PRE)

Electrical conductance through InAs nanowires is relevant for electronic applications as well as for fundamental quantum experiments. Nominally undoped, slightly tapered InAs nanowires were used to study the diameter dependence of their conductance. Contacting multiple sections of each wire, we can study the diameter dependence within individual wires without the need to compare different nanowire batches. At room temperature we find a diameter-independent conductivity for diameters larger than 40nm, indicative of three-dimensional diffusive transport.

For smaller diameters, the resistance increases considerably, in coincidence with a strong suppression of the mobility. From an analysis of the effective charge carrier density, we find indications for a surface accumulation layer.

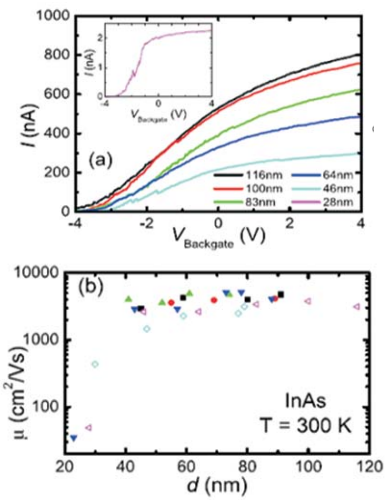

Fig 24. (a) The backgate sweeps for different sections within the same nanowire. The inset shows the data for the section with the smallest diameter. (b) The mobility determined from backgate sweeps. Different symbols correspond to the different devices studied.

Surface passivation of InAs nanowires by an ultrathin InP shell [21] (TUD, PRE)

We report the growth and characterization of InAs nanowires capped with a 0.5-1nm epitaxial InP shell. The low temperature field-effect mobility is increased by a factor 2-5 compared to bare InAs nanowires. The highest low temperature peak electron mobilities obtained for nanowires to this date, exceeding 20 000 cm^2/Vs we also reported.

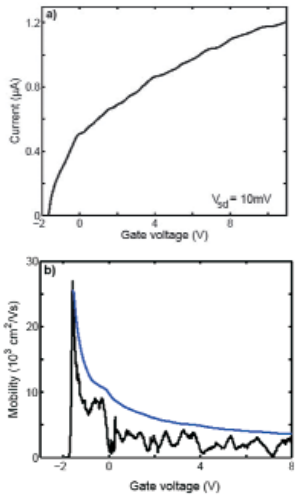

Fig 25. (a) pinch-off curve and (b) extracted field-effect (black) and effective mobilities (blue) of a high mobility core/shell nanowire.

The electron density in the nanowires, determined at zero gate voltage, is reduced by an order of magnitude compared to uncapped InAs nanowires. For smaller diameter nanowires, an increase in electron density was found which can be related to the presence of an accumulation layer at the InAs/InP interface. However, compared to the surface accumulation layer in uncapped InAs, this electron density is much reduced.

We suggest that the increase in the observed field-effect mobility can be attributed to an increase of conduction through the inner part of the nanowire and a reduction of the contribution of electrons from the low mobility accumulation layer. Furthermore it was found that by growing an InP shell around an InAs core, surface roughness scattering and ionized impurity scattering in the accumulation layer is reduced.

1.3.2. Optical studies

Raman and mid-IR spectroscopy (SNS)

A micro-Raman set-up was developed and applied to InAs/InP core-shell structure, as a way to study the strain introduced in the structure and verify the reduced impact of surface states in the capped wires. A clear line width reduction was observed in wires with thick InP shells where less interaction with the surface was expected and a blue shift of the resonances with increasing shell thickness was also detected, which gives indication of the amount of strain in the InAs material.

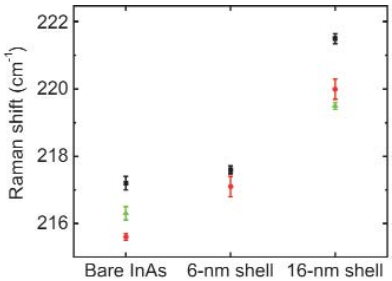

Fig 26. Energy position of the main transverse mode for NWs with different InP shells. Colours are used to distinguish among different wires in the same sample.

Micro photoluminescence studies of single InP nanowires (WU)

The optical study of single nanowires provides important information about physical properties such as size quantization effects. Individual NWs show narrow emission lines with linewidths as low as 2.3 meV which reflects the high structural quality of the nanowires. Blueshifts of the NW emission energy between 25 and 56 meV with respect to bulk InP are related to radial carrier confinement in nanowires with diameters between 15 nm and 50 nm. Time resolved investigations reveal a low surface recombination velocity of 6×10^2 cm/s. [22]

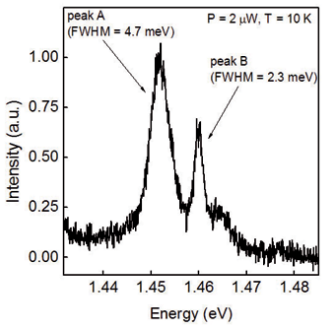

Fig 27. Micro photoluminescence spectrum showing emission from two InP nanowires with narrow linewidths of 4.7 meV and 2.3 meV, respectively.

Study of surface capping of InP nanowires (WU, LU, QM)

Time resolved photo-luminescence spectroscopy was applied to optimize the atomic layer deposition (ALD) of high-κ dielectrics (HfO_2, Al_2O_3) onto InP NWs – a process which typically leads to detrimental surface states. Applying a core/shell growth technique the InP surface quality could be significantly improved in terms of the surface recombination velocity S0 which was reduced to S0 = 9.0×10^3 cm/s in comparison with S0 = 1.5×10^4 cm/s obtained for an untreated reference sample without surface treatment prior to ALD. In an alternative approach, in-situ post-growth annealing in H_2S atmosphere prior to ALD resulted in a nearly fourfold decrease of S_0. These results clearly show the importance of a proper surface treatment prior to oxide capping of III/V NWs for transistor applications.

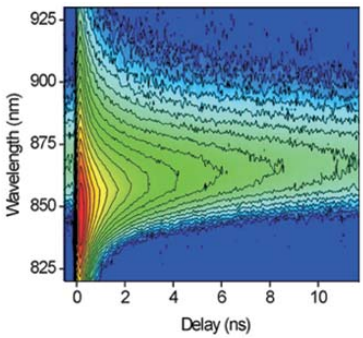

Fig 28. Spectrally and temporally resolved intensity map of the PL emission from HfO_2 capped InP NWs.

1.3.3. X-ray characterization

Study of radial and longitudinal heterostructures (CEA, LU, QuMat)

Quantitative structural information about epitaxial arrays of VLS-NWs have been reported for a InAs/InP longitudinal [23] and core-shell [24] heterostructure grown InAs (111)B substrates. Grazing incidence X-ray diffraction allows the separation of the nanowire contribution from the substrate overgrowth and gives averaged information about crystallographic phases, stacking defects, epitaxial relationships with orientation distributions, and strain. The strain profiles have been

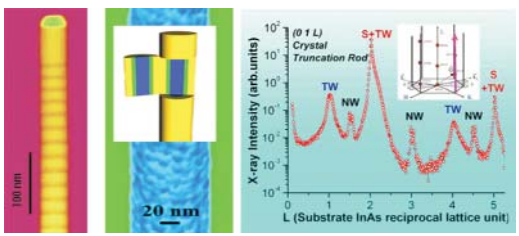

Fig 28. Longitudinal and radial heterostructures measured by Grazing Incidence X-ray Techniques and example of a truncation rod measurement showing the [111] stacking in a longitudinal InAs/InP heterostructure.

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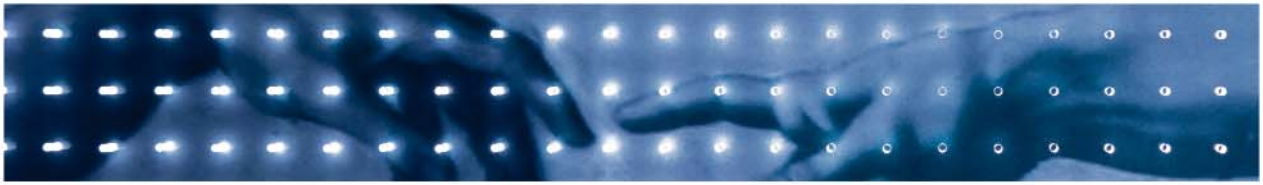

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compared to atomistic and finite element calculations performed at CEA, and Grazing Incidence Small Angles Scattering has been used to extract the shape, diameter and variability of the NWs.

Single object studies (CEA)
The measurement of single NWs with coherent imaging techniques has been developed. This new technique gains insights into the shape of the objects [25], but also into the strain distribution inside one object. Original structural results obtained on sSOI lines with micro-focussed beams have been obtained (unpublished results) as well as the application of this technique to VLS grown samples.

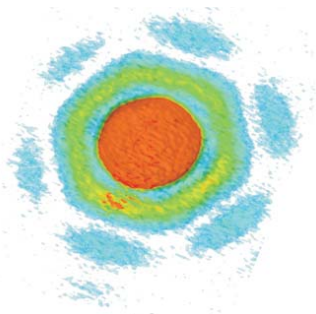

Fig 29. Coherent diffraction of single 95 nm Si nanowire (111) Bragg reflection. The "ab initio" analysis of this pattern allows reconstructing the shape of the NW.

1.3.4. Modelling

Band structure calculations (CEA, LU).
The band structure of group IV and various III-V NWs has actually been investigated in the whole 2-40 nm diameter range. The size dependence of the bandgap energy, subband splittings and effective masses has been discussed in detail [26] and used in collaboration with Lund for the modelling of InAs NW field-effect transistors. [27] Finally, the CEA has investigated the effects of strains on the electronic properties of III-V nanowire heterostructures (e.g., the reduction of the barrier height in tunnel devices). [28]

Transport properties (CEA)
The transport properties of ultimate silicon nanowires with diameters <6 nm has been modeled using quantum Kubo-Greenwood and Green function methods. The impact of surface roughness [29] and dopant impurities on the mobility has been studied. The CEA has shown, in particular, that the impurity-limited contribution to the mobility could be larger in wrap-gate nanowires than in bulk due to the efficient screening of ionized impurities by the gate. Also, the resistance of single impurities can be very dependent on their radial position in the nanowire, leading to significant variability in ultimate devices.

Effect of dielectric environment on the electrical properties (CEA, CNRS/IEMN, LU)
It was shown that the dielectric confinement can be responsible for a significant decrease of the doping efficiency in nanowires. [30] Dopant impurities are progressively "unscreened" by image charge effects when reducing wire diameter, which leads to an increase of their binding energies and decrease of their activity. These predictions have been confirmed by recent experiments by the IBM group. The binding energies of shallow impurities are however very sensitive to the dielectric environment of the nanowires, and can be decreased by embedding the wires in high-κ oxides or wrap-gates. Modelling has confirmed that many electronic properties of semiconductor nanowires are driven more by dielectric than quantum confinement, even in the sub 10 nm range, showing the importance of the "electrostatic" engineering of nanowire devices.

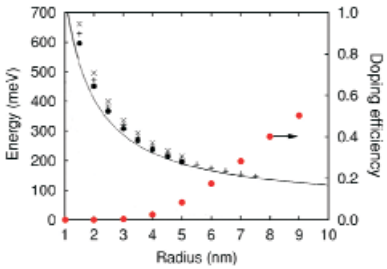

Fig 30. Binding energy of various donors (black symbols, left axis) as a function of the radius R of silicon NWs in vacuum, and room temperature doping efficiency of P donors (red symbols, right axis). The doping efficiency rapidly decreases below R = 10 nm.

1.4. Nanowire devices

1.4.1. InAs FETs

Vertical InAs transistors (LU/QM)
Fabrication of vertical InAs nanowire wrap-gate field- effect transistor arrays with a gate length of 50 nm has been developed. [31] The wrap gate is defined by evaporation of 50-nm Cr onto a 10-nm-thick HfO_2 gate die-

lectric, where the gate is also separated from the source contact with a 100-nm SiO_X spacer layer. For a drain voltage of 0.5 V, a normalized transconductance of 0.5 S/mm, a subthreshold slope around 90 mV/dec., and a threshold voltage just above 0 V were observed.

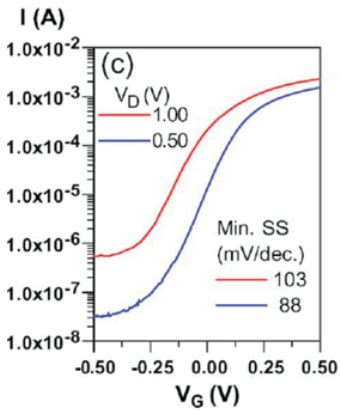

Fig 31. Sub-threshold I-V characteristics of an array of 55 vertical InAs nanowires.

RF characterization of vertical InAs transistors (LU/ QM)

Lund and Qimonda have developed an RF compatible vertical InAs nanowire process, with InAs wires grown on S.I. InP substrates. By combining 70 wires in parallel in a 50Ω waveguide pad geometry, S-parameters (50MHz-20 GHz) for vertical InAs nanowire MOSFETs were measured. A maximum f_t of 7GHz and f_{max}=22GHz [32] was obtained. Small signal modelling allowed for the first extraction of intrinsic device elements forming a hybrid-π equivalent circuit.

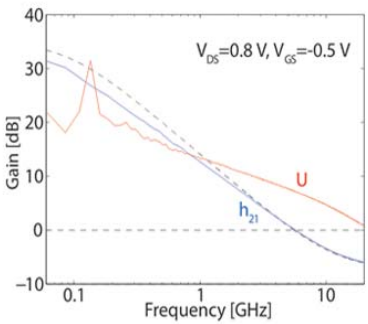

Fig 32. Measured and modelled RF gains for a 90 nm gate length InAs MOSFET.

1.4.2. Other InAs- and III/V-based devices

Nanowire-based multiple quantum dot memory (LU)

We demonstrate an alternative memory concept in which a storage island is connected to a nanowire containing a stack of nine InAs quantum dots, each separated by thin InP tunnel barriers. [33] Transport through the quantum dot structure is suppressed for a particular biasing window due to misalignment of the energy levels. This leads to hysteresis in the charging & discharging of the storage island.

The memory operates for temperatures up to around 150 K and has write times down to at least 15 ns. A comparison is made to a nanowire memory based on a single, thick InP barrier.

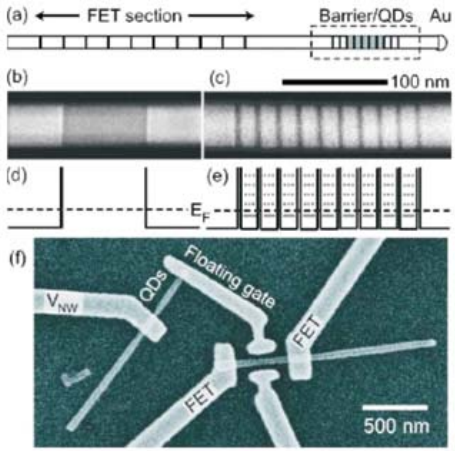

Fig 33. Design and implementation of a multiple quantum dot memory based on nanowires.

Nanowire capacitors (LU)

Vertical InAs nanowire capacitors have been developed based on arrays of nanowires, high-k deposition, and metal deposition. [34] The capacitors show a large modulation of the capacitance with the gate bias, and a limited hysteresis at 0.5 V voltage swing. Via modeling of the charge distribution in the nanowires as a function of the applied voltage, the regions of accumulation, depletion, and inversion have been identified. Finally, the carrier concentration has been determined.

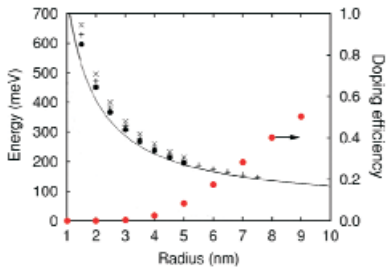

Fig 34. Measured CV profile at 20 MHz.

I.4.3. Si FETs

Doping limits in silicon nanowires (IBM)

The control over doping levels was demonstrated for in-situ doped silicon nanowires using phosphine as the doping source. It was found that the maximum attainable doping is $1\times10^{20}cm^{-3}$ limited by the solid solubility limit of phosphorous in silicon at the growth temperature (450^0C). [35]

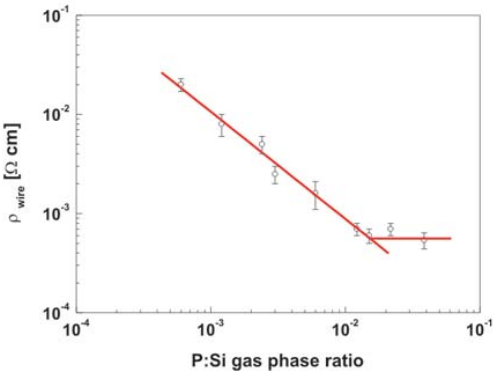

Fig 34. Experimental data of nanowire resistivity vs phosphine concentration. Donor densities up to the solid solubility limit of phosphorous in silicon was achieved.

Doping deactivation (IBM)

It was demonstrated experimentally that dopants inside scaled semiconductors experience a smaller screening as a function of decreasing size leading to a deactivation of the dopants. This effect is caused by a dielectric mismatch between the semiconductor and the surrounding medium. [36]

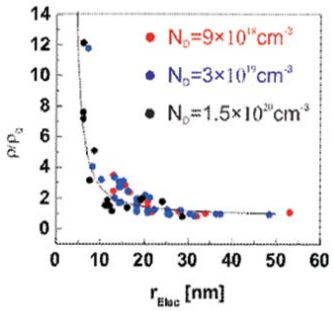

Fig 35. How the resistivity of silicon nanowires increases with decreasing diameter due to doping deactivation caused by a dielectric mismatch between the nanowire core and the surroundings.

Silicon nanowire tunnel FETs (IBM)

Tunnel FETs based on silicon nanowires were demonstrated for the first time. The FET structure was grown by the VLS method and doping was incorporated in-situ. The devices were fabricated in a lateral fashion with both a top and bottom gate. The data obtained on the FETs matched the expected sub-threshold slopes as modeled by a simple WKB approximation. [37]

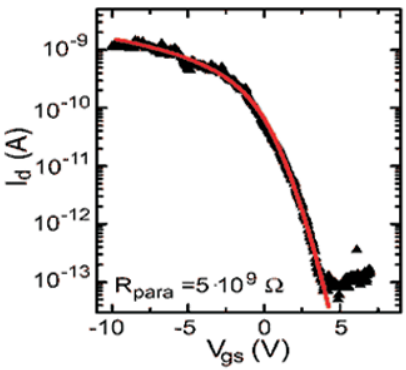

Fig 36. Transfer characteristics of a Si NW tunnel FET with top gate. The red line is calculated using the WKB approximation.

State-of-the-art all-silicon tunnel FETs (IBM)

All-silicon nanowire tunnel FETs with high on-currents were demonstrated. The use of a high-k gate dielectric markedly improves the TFET performance in terms of average slope SS (SS measured between $10^{-7}\mu A/\mu m$ and $10^{-3}\mu A/\mu m$ is 120mV/ dec.) and on-current, I_{on} ($0.3\mu A/\mu m$). The performance of the devices is close to what can be expected from all-silicon tunnel FETs. [38]

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- Taylor's cone can be monitored thanks to a video camera installed in the spraying chamber. Capture of images and video is also possible.
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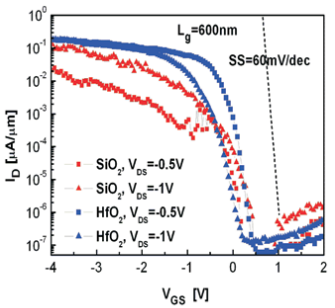

Fig 37. Transfer characteristics of silicon nanowire tunnel FETs with SiO_2 (red) and HfO_2 (blue) gate dielectrics.

Dopant-free polarity control of Si nanowire Schottky FETs (NL)

The accurate and reproducible adjustment of the charge carrier concentration in nanometer-scale semiconductors is challenging. As an alternative to transistors containing doping profiles, dopant-free nanowire transistors have been devised. The source and drain regions are replaced by metal contacts that exhibit a sharp interface to the active region. The current flow is controlled by locally adjusting the electric field at the metal/silicon interface. Independent control of each contact results in transistors that can operate either as p- or n-type. [39]

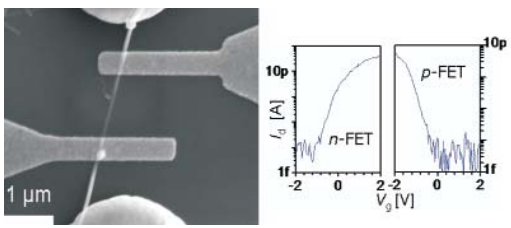

Fig 38. Silicon nanowire FET with two independent top gates, each coupling to a metal/semiconductor junction. The FET can be programmed as p- and n- type.

Complementary logic circuits built from undoped Si nanowire Schottky FETs (NL)

To reduce the static power consumption of digital circuits complementary logic is required. This is enabled by the interconnection between p- and n- type transistors. Complementary nanowire based inverter circuits that do not require doping were developed and characterized. The results show that all logic functions can be performed at low power consumption without dopants. The entire thermal budget for processing is kept below 400°C, enabling a possible future replacement of low mobility organic printed circuits on flexible electronics.

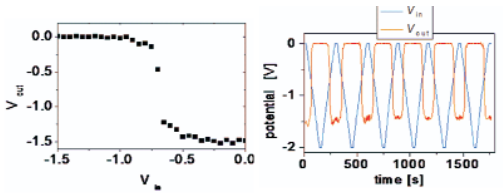

Fig 39. Silicon nanowire inverter characteristics; top: transfer characteristics, bottom: time resolved response.

I.5. Benchmarking and integration

I.5.I. Process upscaling of nanowire growth and devices

Wafer-scale nanowire growth (IMEC)

At first, catalyst-based growth of silicon vertical nanowire using none-gold catalyst systems was considered. Aluminum, which had been shown promising on coupon level tests (UHV-CVD at MPI), proved not up-scalable in the absence of UHV conditions. Indium particles did produce high-yield Si nanowires in PE-CVD but the growth was difficult to control. In view of the many limitations related to Vapor-Solid Liquid growth of silicon nanowires, a seedless (catalyst-free) constrained approach for growing Si and SiGe nanowires onto Si (100) substrates was developed. The growth approach takes advantage of the advances in Selective Epitaxial Growth (SEG) technology to fill the holes without the presence of catalytic metal particles. Nanowires with an intrinsic

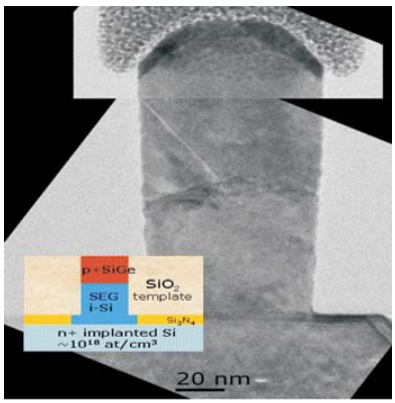

Fig 40. TEM micrograph of a 60nm wide Si/SiGe heterojunction nanowire.

Si segment (channel) and p+ -doped (B) segment of either Si, $Si_{0.85}Ge_{0.15}$ or $Si_{0.75}Ge_{0.25}$ (source) were successfully grown on top of n+-doped (100) substrates. [40]

Large-scale nanowire device integration (IMEC)
IMEC developed an integration flow together with the necessary process modules to fabricate vertical nanowire tunnel-FET devices with wrap-around gates. The nanowires were made by a top-down etch process, however, the integration flow is compatible with a bottom-up approach based on grown nanowires.

Next to the wrap-around gate configuration which provides the best gate control over the channel, a vertical TFET architecture allows a more readily implementation of heterostructures which are needed to boost the tunneling current (see modeling part).

Functional vertical nanowire TFET devices were built on a 200mm wafer platform. [41] Vertical integration implied, among other, the implementation of bottom and top isolation layers, and a amorphous Si capping layer which simultaneously connects the TiN metal gate.

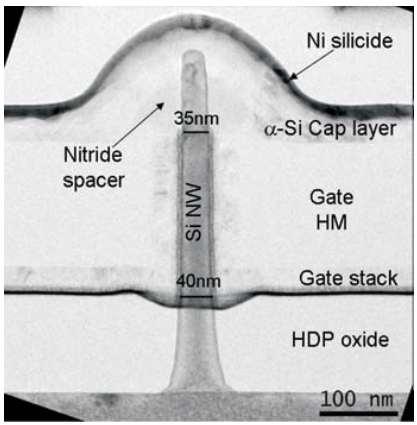

Fig 41. TEM cross-section of the final vertical 35nm NW TFET device (no top oxide isolation) with an advanced a-Si/TiN/HfO_2 gate stack

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Vertical nanowire TFET device (IMEC)
Functional Si nanowire n- and p-TFETs were demonstrated and measured electrically at IMEC using a Kleindiek nanoprober apparatus mounted in a HRSEM. The experimental data are inline with literature data of all-Si Tunnel-FETs. To contributors knowledge, these devices are the first large-scale integrated vertical nanowire devices with state-of-the art high-k metal gate stack. [42]

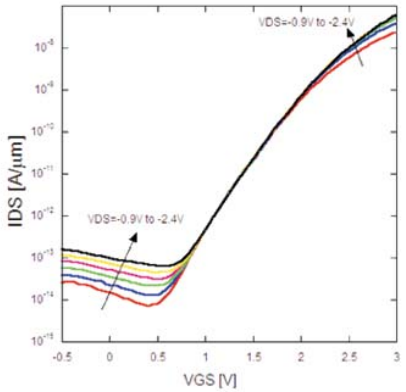


Fig 42. Input I_{ds}-V_{gs} characteristics of the n- TFET device with an epi grown P+ source and a nanowire size of 50 nm on design.

1.5.2. Vertical device architectures and benchmarking

Short-gate and shifted-gate TFET device concepts (IMEC)
It was shown with the help of simulation that the position of the gate can impact the TFET device performance. The advantage of the short-gate TFET are the reduced ambipolar behavior, enhanced switching speed and relaxed processing requirements. [43] When the gate is shifted towards the source-channel a modest increase in on-current can be achieved.

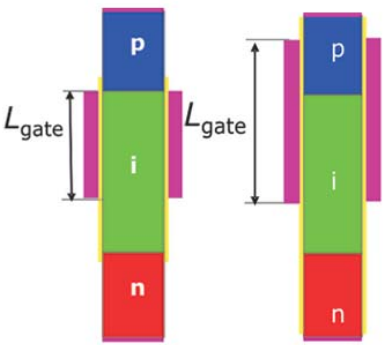


Fig 43. Schematic representation of the short-gate (left) and shifted-gate (right) concepts.

Heterojunction-source TFET (IMEC)
It was shown that the on-current of the TFET device can be increased considerably by placing a foreign source material on top of the Si nanowire channel. Germanium and InGaAs were identified as the source materials of choice for an n-type and p-type TFET device, respectively. The advantage of remaining the Si channel is obvious as conventional Si processing can be used for the gate-stack fabrication. For this work new models needed developed commercial device simulators failed to correctly predict the performance of heterostructure TFETs. [44, 45] Together, the Ge-source for n-type and InGaAs source for p-type, enable a complementary silicon-based TFET suitable for competitive low-power applications. These heterostructure TFET configurations (Ge-Si, InA-Si and $In_{0.6}Ga_{0.4}As$-Si) and their corresponding *I-V* characteristics have been used as input for the circuit simulations by NXP.

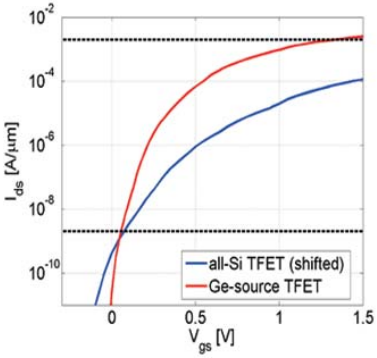


Fig 44. Comparison of I_{ds}–V_{gs} characteristics of all-Si TFET (short gate) and the proposed heterostructure Ge-source Si-TFET, indicating the boost of the current with nearly 2 orders of magnitude to the same level as Si MOSFETs (dashed curves).

1.5.3. Nanowire MOSFETs in the quantum capacitance limit

Quantum capacitance limit for conventional FETs (IBM)
Scaling of NW transistors was investigated by modeling. The important implication of the analysis is that NW with very small diameter enable ultimately scaled transistor devices in a wrap-gate architecture since electrostatic integrity is preserved down to smallest dimensions. However, besides this pure geometrical ar-

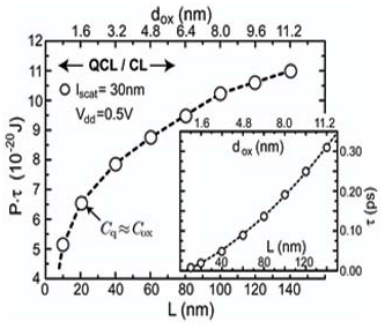
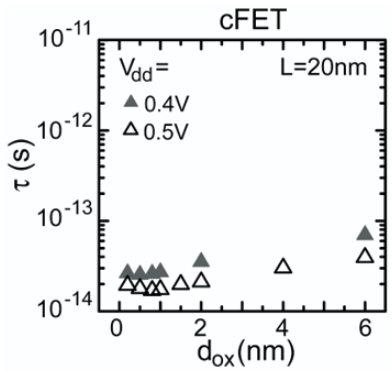


Fig 45. Power delay product and gate delay (inset) versus gate length and oxide thickness for conventional FETs as the transition from classical limit to the quantum capacitance limit is made.

gument the present study shows that NWs offer an additional scaling benefit. In the case of 1D transport, devices can be scaled towards the Quantum Capacitance Limit (QCL) which shows a clear scaling advantage in terms of the power delay product, i.e. the energy needed for switching the transistors. As a result, NWs exhibiting 1D transport are a premier choice as channel material for high performance, ultimately scaled FET devices. [46]

Tunnel FETs in the quantum capacitance limit

Nanowire tunnel FETs versus nanowire MOSFETs (IBM). Modeling of nanowire MOSFETs and tunnel FETs using non-equilibrium Greens functions was used to calculate gate delays as a function of scaling oxide thickness. It was demonstrated that when FETs are scaled to the quantum capacitance limit the tunnel FETs exhibit the same on-state performance as MOSFETs using the gate delay as the performance metric. The on-current is an order of magnitude lower for the TFETs though.



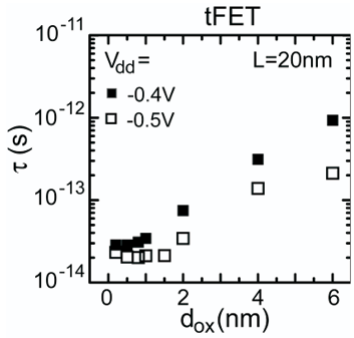


Fig 46. Gate delay versus oxide thickness for nanowire MOSFETs and tunnel FETs.

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2. Overview of nanowire growth

Nanowires can be grown by a variety of methods, but the most common method by far is particle-assisted growth [1, 2] in metal-organic vapor phase epitaxy (MOVPE) or molecular beam epitaxy. This technique uses metal seed particles, most often gold, which act as nucleation centers [3] and direct the growth. The size, number and position of the resulting nanowires are determined by the seed particles, potentially allowing for a high degree of control over the final structures. In this section, patterned growth, heterostructures, doping, crystal structure control, and metal free growth will be briefly reviewed.

The gold seed particles can be deposited in a few different ways. Deposition of aerosol or colloid particles results in more or less randomly positioned nanowires. However, most applications require precise control of the nanowires, both in terms of position and size. Defining the gold particles by electron beam lithography, followed by gold evaporation and lift off, allows for this [4], see Fig. 1.

Formation of heterostructures is at the core of nanowire technology and novel device structures. Three major categories can be identified: axial, radial, and substrate/nanowire heterostructures, e. g. III–V nanowires on Si substrates.

First, axial structures can be formed if the growth precursors are alternated during growth. This results in a variation of the composition along the wire. Furthermore, it is well understood that nanowires represent an ideal system for the growth of axial heterostructures, since mismatched materials can be grown epitaxially on each other without misfit dislocations. This is possible because strain can be relieved by coherent expansion of the lattice outwards (along the wire diameter), avoiding dislocations. Axial heterostructure nanowires were first demonstrated in 1994 for the GaAs–InAs system [5]. Further development of this material system led to reports of high-quality interfaces despite the large lattice mismatch [6]. For the InAs–InP system, atomically sharp interfaces were also reported [7]. Nanowire heterostructure superlattices have been demonstrated for a variety of material systems, with lattice mismatch as high as 3% [8]. Much recent work has focused on attaining sharp heterointerfaces for various material and growth systems. As well, the development of heterostructure nanowires involving ternary compounds such as GaAsP [9], InAsP [10] and InGaAs [11], further increases the potential for applications.

Second, radial structures, also known as core-shell structures, can be formed. In the lateral case, heterostructures are achieved by first growing nanowires by conventional particle-assisted growth, then by changing the growth parameters so that bulk growth is favored. In this way growth on the side facets of the wire will dominate, and shells will form [12].

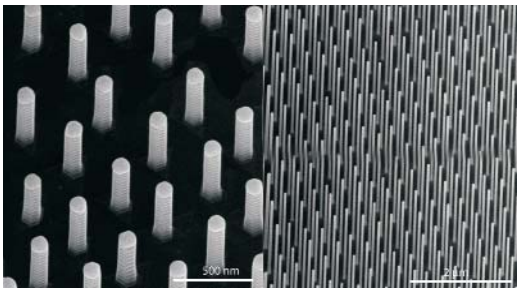

Fig 1. Scanning electron micrographs of gold particle-assisted, MOVPE grown, InAs nanowires in regular arrays, where the positions of the gold particles have been defined by electron beam lithography.

The third category, substrate/nanowire heterostructures, resembles the axial heterostructure with the difference that the substrate is less compliant. Compared to planar heteroepitaxy, the critical thickness for dislocation-free growth becomes considerable larger when strain can be relaxed also radially. This effect enables epitaxy of III–V nanowires on Si [13].

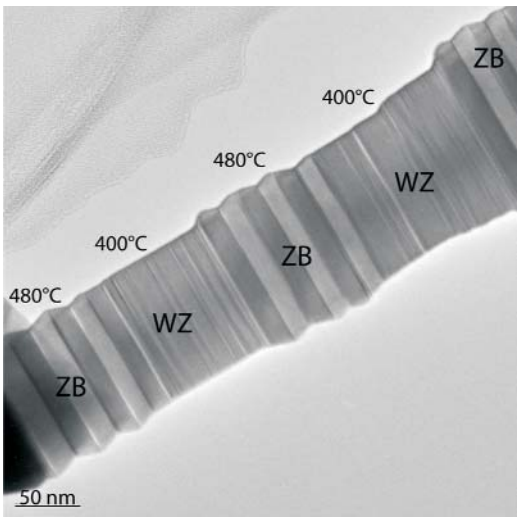

Fig 2. Transmission electron micrograph of a ZB-WZ polytypic superlattice in an InAs nanowire. The structure was achieved by periodically varying the growth temperature.

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For electronics and optoelectronics applications it is necessary to control the conductivity and to be able to fabricate pn-junctions in nanowires. Thus it is of high importance to be able to dope the nanowires; pn-junctions in nanowires have been reported for nitride [14] and other III–V [15, 16] nanowires, even though the incorporation mechanism during particle-assisted growth is not well understood.

Semiconductor nanowires composed of III-V materials such as InAs typically suffer from frequent stacking defects. Although most of these materials exhibit zinc blende (ZB) structure in bulk, nanowires may also be composed of the related wurtzite (WZ) structure. If nanowire growth is not carefully controlled, the resulting structure may consist of a mixture of these two phases, together with twin planes, stacking faults and other polytypes. Various theoretical and experimental works have indicated that uncontrolled structural mixing may be detrimental to electronic and optical properties, and structural variations due to random intermixing may lead to unacceptable variability in material properties. On the other hand, the ability to select between ZB and WZ and to mix these structures in a controlled way may give access to new and exciting physics and applications.

It has recently been shown that the crystal structure of InAs nanowires can be tuned between pure WZ and pure ZB by careful control of experimental parameters, where temperature and nanowire diameter are the most significant [17]. This knowledge enabled the fabrication of twin plane superlattices and ZB–WZ polytypic superlattices in nanowires, see Fig. 2. Twin plane superlattices has also been controllably produced in InP nanowires by the introduction of dopants [18].

Finally, a successful method to grow perfect ZB nanowires that has been reported for GaAs nanowires is to use a two temperature method, where the growth is initiated at high temperature. After this, the temperature is decreased and the main parts of the nanowires are grown at a lower temperature in order to not overcome the energy barrier for twin formation [19]. Quite surprisingly, the same group has recently reported that nanowires free from planar defects can be achieved by growth at high rate [20].

If semiconductor nanowires will be integrated in CMOS compatible processes, as suggested as one possible path to continue the downscaling of electronics, it is necessary to avoid growth from gold particles. Either, other more CMOS compatible metals have to be utilized as seed particles, or particle free nanowire growth has to be relized. Particle free growth from mask openings has been realized in InP [21], GaAs [22], and GaN [23]. Metal free growth has also been realized by growth from self-assembled nucleation templates on organically coated surfaces [24].

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3. Overview transport/optical properties of nanowires[2]

Nanometer-sized quasi 1-dimensional systems, such as semiconducting nanowires (NWs), are attractive building blocks for bottom-up nanotechnology including optoelectronics [1, 2] and manipulation of isolated electron spins [3, 4, 5]. Defect-free nanowire heterojunctions, both longitudinal [6] and radial [7, 8, 9], can be grown due to the small nanowire radius, which allows strain from lattice mismatch to be relaxed radially outwards.

Not only junctions between various different group III-V or IV elements, but even group III-V/IV junctions were reported [10, 11]. InAs is an attractive material because its small bandgap results in a low effective electron mass, giving rise to high bulk electron mobilities (at room temperature 22 700 cm^2/Vs [12] and at low temperature in planar structures over 600 000 cm^2/Vs [13]).

For bulk InAs, it is well known that the surface contains a large number of states that lie above the conduction band minimum and can contribute electrons to form a surface accumulation layer with a typical downward band bending between 0 and 0.26 eV [14]. Because of the large surface charge density, the Fermi level for InAs is pinned in the conduction band, which makes it easy to fabricate ohmic contacts without a Schottky barrier.

This InAs contact property enabled the observation of the superconductivity proximity effect in nanowires [15]. A surface accumulation layer combined with the large surface to volume ratio for InAs nanowires could promise good sensitivity for InAs nanowire sensor applications.

As a fraction of the surface states contributes electrons to the accumulation layer, the InAs surface contains a large number of ionized impurities. Electrons in the accumulation layer therefore experience much stronger ionized impurity scattering than electrons in the inner InAs region. Furthermore, because of the proximity to the surface, surface roughness scattering is also strong. This means that electrons in the surface layer have a strongly reduced mobility compared to electrons in the inner material, typically $\mu surface \sim 4000\ cm^2/Vs$ [12, 14].

For microns thick planar structures of InAs, conduction is dominated by the electrons flowing through the inner region and mobilities are high. The electron mobility is strongly reduced for sub-micron sized InAs structures [12, 14], because of the higher surface-to-bulk ratio. At the same time, the total electron density will increase for smaller thicknesses.

Indications of a surface accumulation layer in InAs nanowires have been observed in [16], where smaller nanowire diameters show an increase in total electron density, consistent with the observations on accumulation layers in bulk InAs [12]. For InN nanowires, magneto-resistance measurements showed Altshuler - Aronov - Spivak (AAS) oscillations, suggestive of shell-like conduction through nanowires [17].

Conduction through InAs nanowires with typical diameters under 200 nm can be expected to be strongly influenced by the presence of a surface accumulation layer. The strong ionized impurity and surface roughness scattering in the surface accumulation layer could explain why InAs nanowires typically have low temperature mobilities of 1000-4000 cm^2/Vs [15, 18, 19, 20]. There have been two reports of InAs nanowires yielding mobilities exceeding 16000 cm^2/Vs [21, 22].

The surface band bending that causes the accumulation layer for InAs is a crystal surface property and the strength of the accumulation is known to be dependent on the surface orientation and termination [14]. Reducing the depth of the band bending will result in a higher relative contribution from the inner electrons to the total conduction and an increase in electron mobility.

An alternative approach to increase electron mobility would be to reduce the scattering in the surface channel by reducing the surface roughness and the scattering on surface states by surface passivation. Natural III-V oxides are soft, hygroscopic, compositionally and structurally inhomogeneous [23,24].

We have extracted the electron mobility from the gate dependence of the current using a simulated nanowire capacitance to the gate. Low temperature mobility has increased by a factor of 2-5 compared to bare InAs nanowires [9]. We also have found among the highest low temperature peak electron mobilities reported to this date, exceeding 25000 cm^2/Vs.

[2] Val Zwiller, and L P Kouwenhoven
Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands

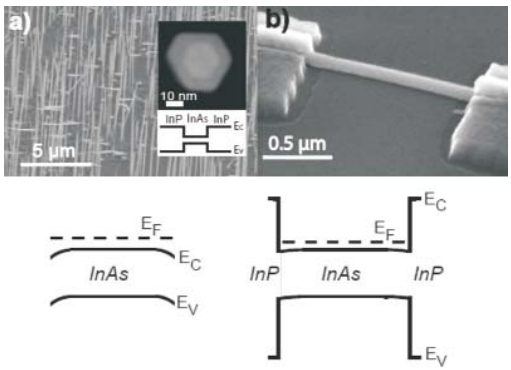

Fig 1. (a) Scanning electron microscope (SEM) image of InAs/InP core/shell nanowires grown on an InP substrate. Inset shows a high angle annular diffraction TEM image of a representative InAs/InP core/shell nanowire. The wire diameter is roughly 20 nm and the shell thickness 7-10 nm. The schematic shows the bandgap alignment for InAs sandwitched between InP. (b) SEM image of a typical nanowire device with Ti/Al contacts as used in our measurements. (c) Schematic of the bandgap bending of an InAs nanowire (a) and an InAs/InP core/shell nanowire.

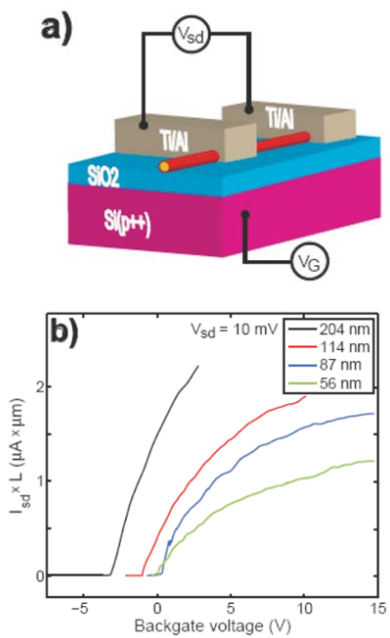

Fig 2. (a) Schematic of a Ti/Al contacted nanowire on a heavily doped Si substrate with SiO2 dielectric. (b) Current through the nanowire as a function of backgate voltage for several NW diameters. Such measurements are used to determine the electron mobility.

To create active photonic elements, the first key step is to incorporate a single quantum dot in a nanowire [25]. Semiconductor quantum dots are well known sources of single [26, 27] and entangled photons [28, 29, 30] and are naturally integrated with modern semiconductor electronics. Incorporation in semiconducting nanowires brings additional unique features such as natural alignment of vertically stacked quantum dots to design quantum dot molecules and an inherent one-dimensional channel for charge carriers. Furthermore, the unprecedented material and design freedom makes them very attractive for novel opto-electronic devices and quantum information processing.

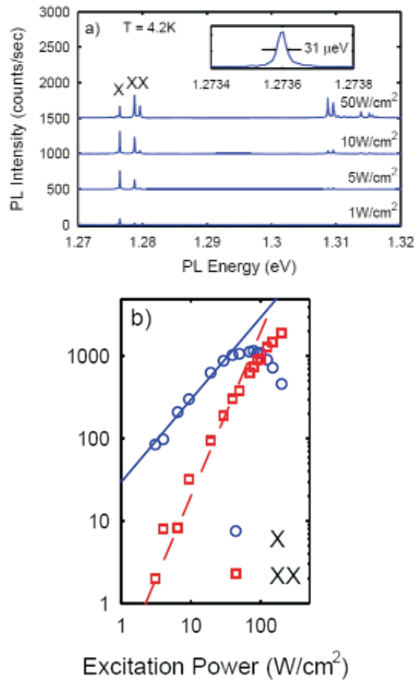

Fig 3. (a) Power dependence of the photoluminescence from a single quantum dot in a nanowire under continuous excitation at 532 nm. (b) Integrated power dependence of two narrow emission lines attributed to the exciton and biexciton. Samples grown by the Bakkers group.

Access to intrinsic spin and polarization properties of a quantum dot in a nanowire is challenging because of the limited quality of nanowire quantum dots, partly because the quantum dot is located very close to the sample surface. Moreover, the nanowire geometry strongly affects the polarization of photons emitted or absorbed by a nanowire quantum dot, and is thus an important obstacle for applications based on intrinsic spin or po-

larization properties of quantum dots such as electron spin memory or generation of entangled photons. It has been shown that photoluminescence of homogeneous nanowires is highly linearly polarized with a polarization direction parallel to the nanowire elongation.

In Fig. 3(a) we show a typical excitation power dependence revealing a usual exciton-biexciton behavior and a p-shell at 30 meV higher energy. The inset shows the narrowest emission we have observed to date with a FWHM of 31 μeV, limited by our spectral resolution. The integrated photoluminescence intensities of the exciton and biexciton as a function of excitation power, represented in Fig. 3(b), show that the exciton (biexciton) increases linearly (quadratically) with excitation power and saturates at high excitation powers. This behaviour is typical for the exciton and biexciton under continuous excitation.

The nanowire geometry is not the only source of polarization anisotropy. Calculations by Niquet and Mojica [31] show that the polarization properties are strongly affected by the aspect ratio of the quantum dot dimensions, due to strain originating from the lattice mismatch between the nanowire and the quantum dot. However, in our case the strain is negligible due to the low phosphorus content and the main contribution to polarization anisotropy stems from the nanowire geometry.

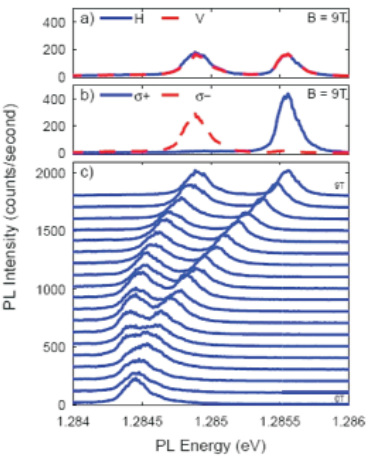

Fig 4. (a) and (b) Polarization sensitive photoluminescence of a standing nanowire quantum dot at 9 T. The solid (dashed) curve in (a) represents vertical (horizontal) linearly polarized exciton emission, denoted by H (V). The solid (dashed) curve in (b) represents left- (right-) hand circularly polarized exciton emission. (b) PL of a standing nanowire quantum dot under external magnetic field. Magnetic field is varied between 0 and 9 T in steps of 0.5 T. Sample grown by the Bakkers group (Philips).

Standing nanowires enable the extraction of any polarization with equal probability. This enables the observation of Zeeman splitting, provided that the emission linewidth is narrow enough. In Fig. 4(a) we show a magnetic field dependence of the exciton emission measured on a standing InP nanowire containing an InAsP quantum dot. The nanowire was grown by MOVPE using colloidal gold particles as catalysts by the Bakkers group. Polarization studies at 9 T show circular polarization Fig. 4(b) and no linear polarization Fig 4(a).

One challenge is to obtain good ohmic contacts to the p doped side of a nanowire LED. In Fig. 5 the device-layout, the nanowire LED emission and the electrostatic potential distribution along the device are shown. The junction is readily visible by transmission electron microscopy, the modification in doping brings about a modification of the nanowire diameter. Electrostatic force measurements are shown on the right of Fig. 5, under a reverse bias of 1.5 V, a prominent drop in potential is observed at the expected position of the pn junciton. Under zero and 1.5 V forward bias, no potential drop is observed on the pn junction, this demonstrates the presence of a pn junction in the contacted nanowire and shows that the contacts are ohmic.

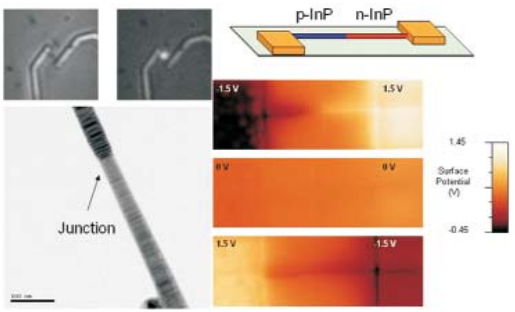

Fig 5. Single nanowire light emitting diode. Left: microscope image of the nanowire LED without and with forward bias. Bottom left: TEM image of a pn junction in an InP nanowire. Right: electrostatic force measurements under forward (top) and reverse (bottom) bias.

An electrically contacted nanowire can also be used for photodetection, as shown in figure 6. Fig. 6 left shows the photocurrent intensity as a function of applied bias in the dark and under illumination. Fig. 6 right shows the polarization dependence of the photocurrent for a lying nanowire as a function of the laser linear polarization angle. The observed photocurrent polarization is in agreement with the polarization ratio measured by photoluminescence.

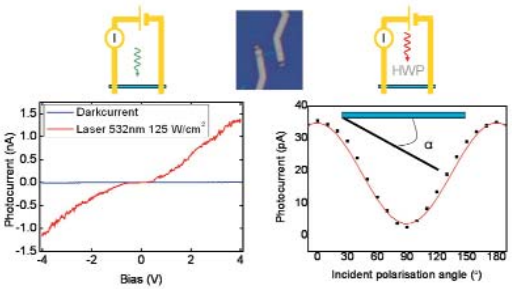

Fig 6. Photocurrent measurement on a single nanowire. Left: photocurrent as a function of applied bias. Right: photocurrent as a function of laser polarization.

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Valery Zwiller, Hans Blom, Per Jonsson, Nikolay Panev, Soren Jeppesen, Tedros Tsegaye, Edgard Goobar, Mats-Erik Pistol, Lars Samuelson, Gunnar Bjork, Appl. Phys. Lett 78, 2476 (2001)

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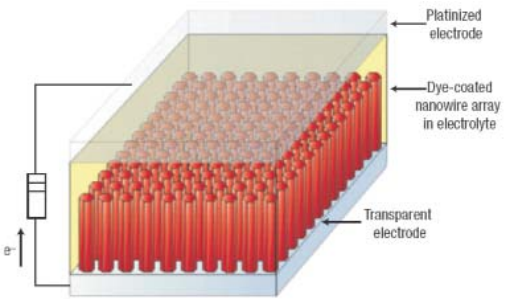
4. Nanowires for energy applications

Several possibilities exist for the use of nanowires in the energy sector. This includes three categories: a) energy saving, b) energy harvesting, and c) energy storage. Within category a) we see two main research areas: lower power-consuming electronics and low-power illumination by solid-state lighting.



Schematic of a nanowire array for solar cell application.

Nanowire FETs are regarded as one of the emerging nanoelectronic devices [1]. Low-power memory cells (so-called tunneling SRAMs) have already been demonstrated [2] as well as low-power tunnel FETs [3]. Additionally, vertically wrap-gated InAs nanowire devices with subthreshold slope around 90 mV/dec have been realized [4].

Besides electronic devices with lower power consumption, the thrive goes towards solid-state lighting devices for replacement of incandescent light bulbs and fluores-

cent lamps. A number of groups are working to realize this goal using nanowire structures. As early as 1994, light-emitting diode structures of GaAs nanowires with pn-junctions had been reported by the group of K. Hiruma at Hitachi [5]. First ten years later, similar devices had been demonstrated in nitride nanowire structures [6]. The fabrication of InP-InAsP nanowire LED structures where the electron-hole recombination is restricted to a quantum-dot-sized InAsP section has also been reported making these devices promising candidates for electrically driven quantum optics experiments [7].

Arrays of nanowire light-emitting structures in the GaAs-InGaP were realized in cooperation between academic and industrial research in 2008 [8]. High brightness GaN nanowire LEDs emitting in the UV-blue region have been demonstrated [9] andnitride-based LED arrays have recently been reported [10].

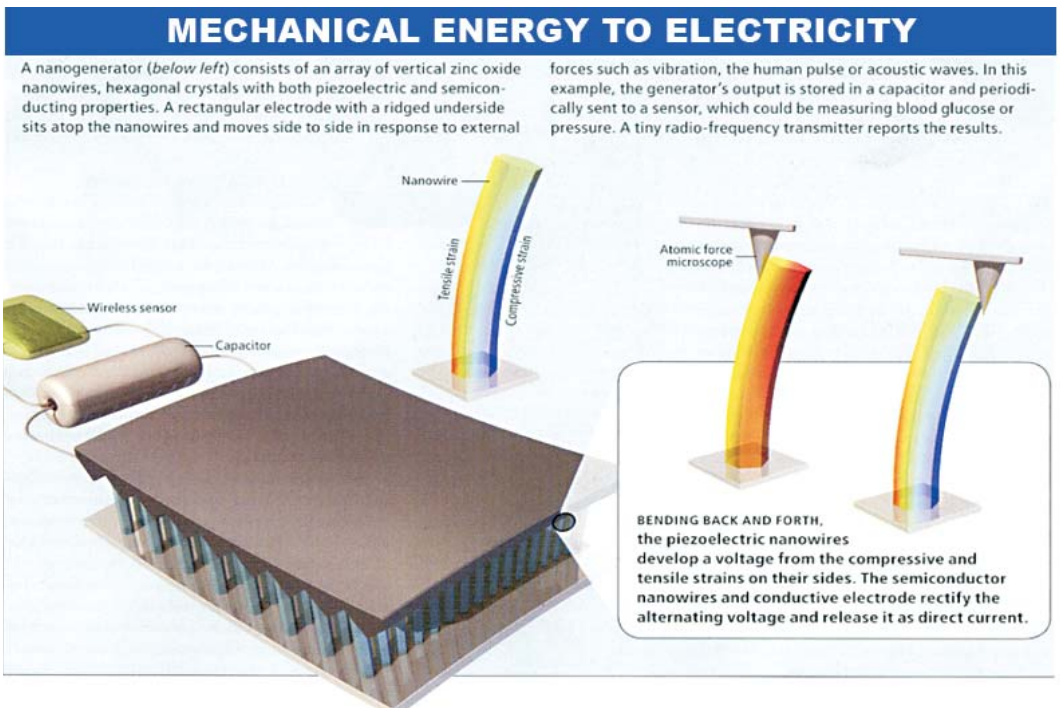
Three research areas can be identified within category b) energy harvesting: conversion of light, heat or movement into electricity. For harvesting of light several nanowire materials have been and are investigated.

P. Yangs group at Berkeley realized a dye-sensitized solar cell architecture in which the traditional nanoparticle film is replaced by a dense array of oriented and crystalline ZnO nanowires [11].

Using silicon, by a simple chemical etching technique-nanowire solar cell structures have been realized with poor performance [12] and p-i-n coaxial silicon nanowire solar cells have been reported with a conversion efficiency of 3.4% under illumination of one sun by the Lieber group from Harvard [13].

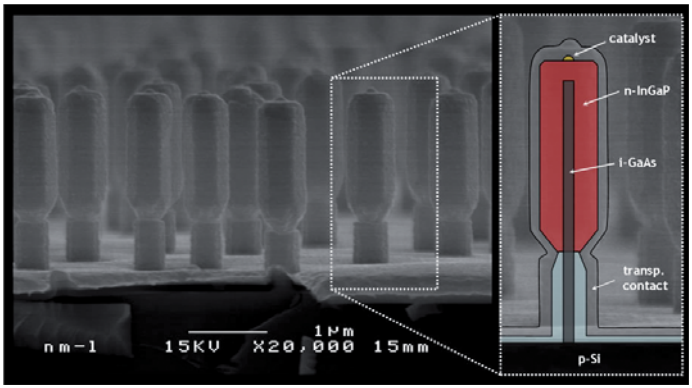
Silicon wires embedded in a polymeric film with potential to achieve high efficiency have recently been demonstrated [14] and even global players like General Electric Inc. show interest in silicon nanowire solar cells [15]. Solar cells have been realized with arrays of CdS nanowires grown on Al substrates and embedded in CdTe matrix showing a conversion efficiency of 6% [16].

Periodically aligned InP nanowires with pn-junctions have been reported with solar power conversion efficiency of 3.4% [17]. Other efforts on III-V nanowire



Schematic of piezoelectric energy conversion with nanowires.

solar cell structures are conducted within the EU-project AMON-RA [www.amonra.eu], where so far pn-junctions in InP nanowires have been demonstrated [18].
Some effort is going on to realize thermoelectric devices with nanowire structures, so far, mainly on a theroretical level [19]. However, first experimental studies have been conducted [20]. An interesting approach is the conversion of mechanical energy in electricity using the piezoelectric properties of ZnO nanowires [21].



Nanowire array with light-emitting structures.

For the last category where nanowires could be used in the energy sector, energy storage, we are not aware of any ongoing research.

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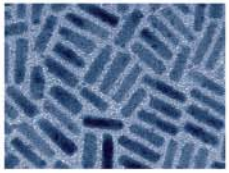
MOLECULAR NANOSCIENCE



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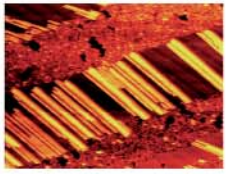

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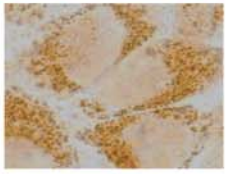
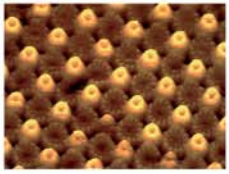
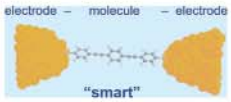


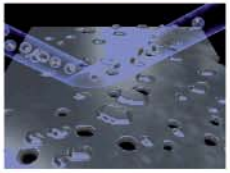
NANOBIOSYSTEMS: BIOMACHINES AND MANIPULATION OF MACROMOLECULES



NANOELECTRONICS AND SUPERCONDUCTIVITY



SEMICONDUCTING NANOSTRUCTURES AND NANOPHOTONICS



HORIZONTAL PROGRAM ON NANOFABRICATION AND ADVANCED INSTRUMENTATION

IMDEA-Nanociencia is a private Foundation created by joint initiative of the regional Government of Madrid and the Ministry of Education of the Government of Spain in February 2007 to manage a new research Institute in Nanoscience and Nanotechnology (IMDEA-Nanociencia), which is located in the campus of the Universidad Autónoma de Madrid, 12 km away from Madrid downtown with an excellent communication by public transportation with the Madrid-Barajas airport (25-30 min) and Madrid downtown (15-20 min).

The Institute offers attractive opportunities to develop a career in science at various levels from Ph.D. students to senior staff positions.

Contact

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5. Overview of nanowires for biology/medicine

Nanowires have a size scale that overlaps with fundamental building blocks of cells. That makes them particularly suitable for biological and medical applications. Here we list a few examples of promising applications in our field of interest.

Neural network on a chip

Neural networks on a chip have many applications in neuroscience. The ability to control the cell position and the connections between cells can yield new knowledge on interactions between neurons and is a crucial component in the development of next-generation prostheses. Axonal guidance can be achieved using chemical or topographical modifications on the surface [1, 2]. Parallel rows of nanowires have proven to provide an excellent way of controlling cell growth and guidance of regenerating axons [3]. The rows of wires act as fences, confining the axons. The small radii of the wires prevent the axons from climbing the nanowires as the growth cone always encounters the wires at a 90° angle in contrast to micro structured walls, where fibers can reach the top of the wall by climbing at an intermediate angle.

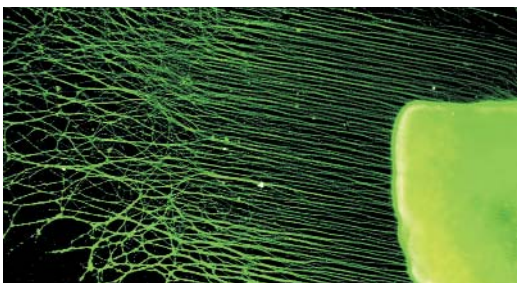

Fig 1. Fluorescence microcopy image of a superior cervical ganglion growing on a 1 x 1 mm^2 area with rows of GaP nanowires. The axons are guided with high fidelity by the rows of nanowires.

To be able to independently address two populations of axons on a chip surface, the different populations must be fully separated. This can be achieved by a ratchet pattern consisting of short rows of nanowires that rectify the axonal outgrowth [4].

Nanowires may thus provide a basis for advanced control of neuronal growth on a chip, where a large range of functionalities can be implemented, including chemical sensors and electrodes to investigate neuronal function at high temporal and spatial resolution.

Cellular force measurements using nanowire arrays

Cellular mechanotransduction is a rapidly growing field with recent studies showing that external and internal forces can alter cellular signaling and function [5, 6]. There are many ways to measure cellular forces in vitro. Optical tweezers and micropipettes are capable of probing picoNewton forces. While being very sensitive, these techniques can only measure forces at a few points simultaneously in a cell. With an elastic substrate cellular forces can be measured in an ensemble of cells [7]. This method, as well as its derived method based on elastomer micro-pillar arrays can measure forces from nanoNewton up to hundreds of nanoNewton [8, 9]. However, the spatial resolution of these methods is limited by the size of the pillars and/or markers to 2 µm at

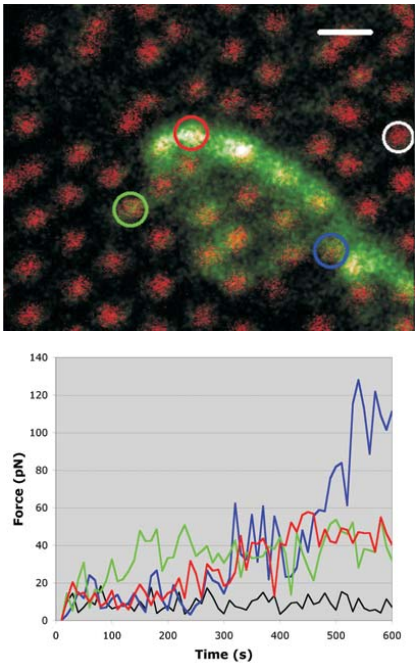

Fig 2. Cellular force measurements using nanowire arrays. (LEFT) Confocal fluorescence image of a growth cone on 40 nm diameter 5 µm long nanowires. Scale bar 1 µm. (RIGHT) Forces exerted on the nanowires highlighted in the left images. The forces range from 20 to 130 pN.

the very best. Nanowires, on the other hand, with their high aspect ratio and small diameter have a great potential for detecting small forces with high spatial resolution, limited by the achievable density of the nanowires to about 1 µm. Using an array of 40 nm diameter and 5 µm long nanowires, force measurement down to 20 pN has been demonstrated on growth cone lamelipodia [10], consistent with data obtained using optical tweezers on the same system [11]. The results show that nanowire arrays can be used as a sensitive force probe that has the advantage of allowing simultaneous measurements with high probe density and high spatial resolution.

Hollow nanowires

The controlled transfer of specific molecules into (and out of) cells is a fundamental tool in cell biology. Electroporation is widely used in bulk and on single cells. However, it merely opens up a conduit for diffusional transport into or out of the cell. Microinjection have been developed to provide a more controlled and selective transport into single cells [12].

Large needles require very slow movement of the needles to allow the adaptation of the cytoskeleton [13, 14]. Decreasing the size of the needle to the nanoscale minimizes any deleterious effect on the cell. Furthermore, arrays of needles can be defined on a flat substrate for massively parallel single-cell experiments.

One example involves the binding of plasmid DNA to the nanoneedles and the subsequent impalfection of cells with a gfp-coding plasmid [15]. Another example involves hollow nanowires that are filled with the molecule of interest and used similarly [16]. In both cases the wires are preloaded and used only once and furthermore rely on passive release in the cytosol. Hollow nanowires connected to an external fluidics system avoid these limitations. By combining such nanowires with a microfluidic system for cell capture, an array of individually addressed cells can be created with potential applications in systems biology, neurobiology, tissue engineering and stem cell differentiation.

Nanowire-based biosensors

Semi-conductor nanowire field effect transistors are a very sensitive tool for detection of biomolecules. The binding of analyte molecules to immobilized DNA or antibody probes may result in a change in the surface charge, thereby changing the nanowire conductance. This method has been used successfully to detect single viruses, cancer markers, and proteins [17-19].

Nanowire-based electrodes for neural interfaces

The development of neural interface is a rapidly growing field. Standard neural electrodes have sizes in the micrometer range and their implantation triggers a strong inflammatory response that often makes it necessary to remove the electrode. It has been shown that carbon nanotubes at the surface of neural electrodes improve the electrical properties of the electrodes and elicit a lower tissue inflammatory response [20].

Carbon nanotubes form a very strong seal with the neurons, which is also expected to be the case using nanowires. Nanowire field effect transistor arrays have been

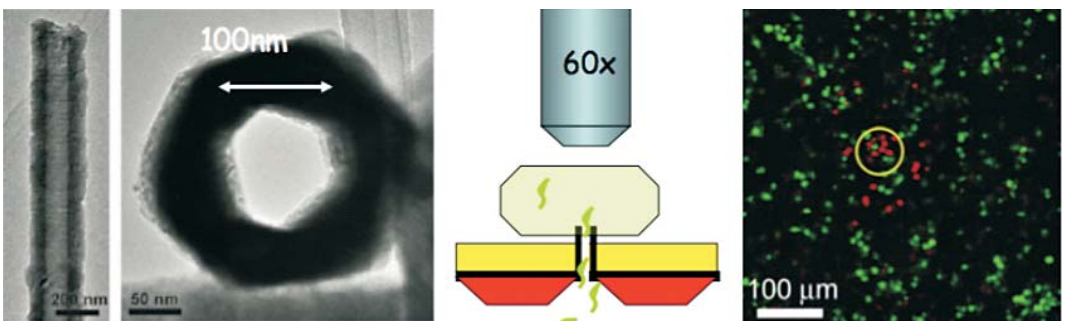

Fig 3. Hollow nanowires for molecular transport. (LEFT) Initially GaAs/Al_2O_3 core/shell nanowires are grown. Subsequently the GaAs core is etched resulting in a hollow Al_2O_3 nanowire. (CENTER) Schematic of a cell impaled by a nanowire with molecules diffusing from the bottom reservoir. (RIGHT) Macrophages expressing GFP on a surface. Where the hollow nanowires establish a connection across the device, membrane impermeable propidium is injected by diffusion into the cells.

used to form nanoscale junctions with axons and dendrites of neurons cultured on the array. The nanowire transistors could stimulate and inhibit neuronal signals, as well as measuring their amplitude and firing rate [21].

It has been shown that neurons can grow and thrive on vertical nanowire substrates [15, 22]. The cell survival was higher on nanowire substrates compared to controls (growth on flat surfaces) despite the fact that the cells were penetrated by the nanowires. This suggests that nanowire-based electrodes will form tighter junctions with the neurons and therefore will record or stimulate more efficiently. In this context, new electrodes consisting of vertical nanowires on the surface of a microelectrode are being developed for brain implantation purposes.

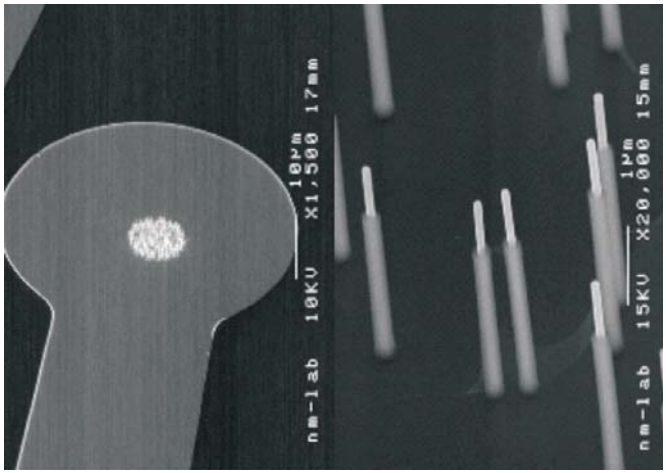

Fig 4. Scanning electron micrograph of nanowire-based electrodes.

Such nano-electrodes could communicate with multiple individual neurons in the brain on a long-term basis. The possible applications are diverse, ranging from fundamental studies of mechanisms of learning to therapeutic treatment of Parkinson's disease.

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Annex I

I. Report from the NODE workshop on nanowire electronics

During the days September 23-24, 2009, was organized in Lund the "NODE Workshop on Nanowire Electronics" which was both a dissemination event of the four years of the Integrated Project NODE ("Nanowire-based One-Dimensional Electronics"), and an opportunity for this research field to obtain sharp feed-back from a set of highly knowledgeable invited keynote speakers.

The focus was on four key issues for the field: one session on "Wrap-gate Transistors", for which we were pleased to have as external keynote speakers Wilfried Hänsch from IBM Yorktown Heights, talking primarily about planar wrap-gate transistors and circuits, and Matthias Passlack from TSMC-Europe in Leuven, talking primarily about comparisons between traditional CMOS and the opportunities from integration of III-V wrap-gate transistors with silicon technology. Added to these presentations where two reports from the NODE research, by Claes Thelander from Lund and Mikael Björk from IBM Zurich.

In the second focused session, on "Ultra-low Power Devices" the keynote presentation was given by Joachim Knoch from TU Dortmund, talking primarily on the potential of Tunnel FETs for ultra-low power applications, with a special focus on what can be achieved in terms of ultra-steep sub-threshold slopes. Two internal NODE presentation were also made here, by Anne Verhulst at IMEC Leuven and Heike Riel from IBM Zurich.

In the third focused session, we looked at opportunities for "Other Nanowire Applications", which primarily in the program meant applications for Memories and RF-applications. The external keynote speaker, Thomas Mickolajick from Freiberg University focused on Memory applications and how nanowire technology can come to contribute to this development. From the NODE research was reported by Walter Weber from the Namlab in Dresden and by Erik Lind from QuMat Technology.

In the fourth of the focused sessions, on "Integration Issues", Hugo De Man from IMEC, Leuven gave an overview of the field and pointed out the challenges that a

new technology has to face to compete with CMOS. He also stressed the value of not limiting the assessment of what nanowires can bring to only ICs, but also to focus on the "More than Moore" opportunities offered. In this session, the state-of-the-art as has been reached in NODE was reported by Philippe Vereecken from IMEC Leuven.

The concluding session was based on a panel discussion with contributions from Lars Tilly (Ericsson Research), Wilfried Hänsch (IBM), Hugo De Man (IMEC) and Matthias Passlack (TSMC), and was introduced and moderated by Lars-Erik Wernersson from Lund. Many different topics were covered, including the pull from systems industry, like mobile phone applications, the issues of integration of a new technology with mainstream silicon technology, and comparisons between the situation for this field of R&D in Europe in a comparison with the USA, where quite different traditions and conditions lead to a more optimal development of the field.

- **Hugo De Man:** "As a conclusion I propose that, if we want to investigate nanowire TFETs as a possible low power device after ultimately scaled CMOS, a *multidisciplinary* project on *Systemability of future technologies* should be launched where process, physics team up with circuit and system people. Otherwise we get stuck in the famous *'European Research Paradox'* where we complain about the fact that excellent research does not lead to true innovation i.e. its translation of it in industrially relevant results.

  Finally perhaps a bit too much focus is on nanowires as a successor for CMOS logic or RF circuits. As was noted by TSMC there is also the trend towards *More than Moore* technologies that will play a dominant role in the world of *Ambient Intelligence* by complementing the intelligent CMOS part with nomadic communication and nanotech interfaces to the living and non-living world. Thereby *novel functionality* such as sensors, actuators, optical interfaces, resonators etc. is needed. Nanowires can provide novel solutions in this field."

- **Matthias Passlack:** "Feature size scaling which has been driving CMOS throughout the last decades will increasingly be complemented by other advancements on the device and system level. Transistor trends include use of high-k dielectrics, multi- and wrap around gate architectures, strained layers, heterostructures, and new channel materials. III-V semiconductors with their high carrier (electron) mobility, direct bandgap functionality, and flexibility for heterostructure design have recently garnered increasing attention. The III-V nanowire appears to be a universal vehicle addressing many of the above aspects including high electron mobility channel, wrap around gate, direct bandgap, and heterostructure design. Moreover, nanowires provide new avenues for high crystal quality in highly lattice-mismatched systems such as III-V semiconductors on silicon substrate. For example, III-V nanowires could be the efficiency RF components and light emission devices monolithically integrated on a silicon substrate."

2. Report on the Nanowire Growth Workshop 2009 (NWG2009)

Introduction

NWG2009 (Paris, 26-27 october 2009 was the 4th edition of an international meeting highly focused on semiconductor nanowire growth. The workshop was first held in Lund (2006 and 2007) and then in Duisburg (2008). This year, the workshop was organized in Paris and lasted two days. It brought together 116 researchers from 19 countries. The workshop program comprised six invited talks, 19 orals and 48 poster presentations. This sizable and active participation indicates that many issues are still to be addressed to improve the control of nanowire growth, which is much more complex than two-dimensional layer growth. In return, the researchers expect much more flexibility to fabricate original nano-objects which will allow investigating the physics of one-dimensional systems or designing new devices with improved performances.

Steering committee of Nanowire Growth Workshop

Eric Bakkers
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Knut Deppert
Solid State Physics, Lund University, Lund, Sweden
Anna Fontcuberta y Morral
Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland

Lutz Geelhaar
Paul-Drude-Institut für Festkörperelektronik, Berlin, Germany
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Stephen D. Hersee
University of New Mexico, Albuquerque, USA
Michael Heuken
Aixtron, Aachen, Germany
Kenji Hiruma
Hokkaido University, Sapporo, Japan
Faustino Martelli
IMM-CNR, Roma, Italy
Werner Prost
Universität Duisburg-Essen, Duisburg, Germany
Helge Weman
Norwegian Univ. of Science and Technology, Tronheim, Norway
Margit Zacharias
Universität Freiburg, Freiburg, Germany

NWG2009 organizing committee

Jean-Christophe Harmand CNRS-LPN, Marcoussis, France
Frank Glas CNRS-LPN, Marcoussis, France
Véronique Thierry-Mieg CNRS-LPN, Marcoussis, France

Keywords

Nanowires; Crystal growth; Elementary semiconductors; Compound semiconductors; III-V on Si
Cristalline structure; Catalyst; Structural properties; Crystal defects; Morphology; Surface energies; Doping, p-n junctions; Growth modeling; Self-assembling

Program of NWG2009

Invited speakers

S. Kodambaka, Department of Materials Science and Engineering, University of California Los Angeles, Los Angeles, USA
Growth of silicon nanowires using AuAl alloy catalysts

V. Schmidt, Max-Planck-Institut für Mikrostrukturphysik, Halle, Germany
Aspects of silicon nanowires growth

K. Kishino, Department of Engineering and Applied Sciences, Sophia Nanotechnology Research Center, Sophia University, Tokyo, Japan
Blue to red emission InGaN-based nanocolumns and related technology

R. R. LaPierre, Centre for Emerging Device Technologies, McMaster University, Hamilton, Canada
Fundamental issues in MBE-grown nanowires for device applications

M. Galicka, Institute of Physics, Polish Academy of Sciences, Warsaw, Poland
III-V nanowires of wurtzite structure
P. Caroff, Institut d'Electronique, de Microélectronique, et de Nanotechnologie, Villeneuve d'Ascq, France
Tuning crystal structure in III-V nanowires

Oral contributions

F. Li, Department of Materials, University of Oxford, Oxford, United Kingdom
Doping-dependent nanofaceting on silicon nanowire surfaces

T. Xu, Institut d'Electronique, de Microélectronique et de Nanotechnologie, Villeneuve d'Ascq, France
Atomic scale structure of <III>-oriented Si nanowire

N. J. Quitoriano, Mining and Materials Engineering Department, McGill University, Montreal, Canada
Engineering Si and Ge nanowire growth direction

I. Zardo, Walter Schottky Institut, Technische Universität München, Garching, Germany
Silicon nanowires growth using gallium and indium as catalysts

K. Naji, Institut des Nanosciences de Lyon, Ecole Centrale de Lyon, Ecully, France
Defect free InP NWs on SrTiO3 substrates grown by VLS-assisted molecular beam epitaxy

T. Gotschke, Institute of Bio- and Nanosystems, Forschungszentrum Jülich, Jülich, Germany
Doping effects of MBE-grown InN NWs by means of Si and Mg

M. Knelangen, Paul-Drude-Institut für Festkörperelektronik, Berlin, Germany
Strain relaxation and nucleation mechanisms of self-induced GaN nanowires

E. Bellet-Amalric, Nanophysics and Semiconductors Group, INAC and Institut Néel, Grenoble, France
Insertion of CdSe quantum dots in ZnSe Nanowires: MBE growth and microstructure analysis

A. Hayashida, Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo, Japan
Fabrication of a GaAs quantum well embedded in AlGaAs/GaAs hetero-structure nanowires by selective-are MOVPE

M. T. Borgström, Solid State Physics, Lund University, Lund, Sweden
Decoupled axial and radial nanowire growth by in-situ etching

V. G. Dubrovskii, St.-Petersburg Physics and Technology Centre for Research and Education, Russian Academy of Sciences, St.-Petersburg, Russia
Self-consistent theory of nanowire growth and crystal structure

J. Johansson, Solid State Physics, Lund University, Lund, Sweden
Wurtzite–zinc blende transition in InAs nanowires

B. Mandl, Institute for Semiconductor and Solid State Physics, University Linz, Austria
Time dependence of Au-free InAs nanowire growth

R. E. Algra, Materials Innovation Institute, Delft, The Netherlands
Correlated twins in nanowires

H. Shtrikman, Braun Center for Submicron Research, Weizmann Institute of Science, Rehovot, Israel
High quality InAs nanowires grown by VLS assisted MBE

H. J. Joyce, Department of Electronic Materials Engineering, Australian National University, Canberra, Australia
Optimising GaAs and other III–V nanowires

E. Gil, Laboratoire des Sciences et Matériaux pour l'Electronique et d'Automatique, Université Blaise Pascal, Clermont-Ferrand, France
Rodlike GaAs nanowires with exceptional length

Highlights of the workshop

Gold remains the most popular catalyst used to assist semiconductor nanowire formation. Alternative metals have been presented which can modify the growth kinetics, the nanowire morphologies and their structure. In particular, catalyzing Si/Ge nanowire growth with (Au,Al) alloy particles tends to favour the vapour-solid-solid (VSS) mode, which produces sharper interfaces in Si/Ge heterostructures (S. Kodambaka, University of California, Los Angeles, USA). An overview of the expected growth mode - vapour-liquid-solid (VLS) or VSS - for a large panel of metallic catalysts has been presented by V. Schmidt (Max-Planck-Institute für Mikrostrukturphysik, Halle, Germany).

An interesting influence of the proximity of oxides on nanowire growth has been demonstrated. N. J. Quitoriano (Hewlett-Packard Laboratories, Palo Alto, USA) showed that nanowire growth can be guided by the SiO_x surface of pre-patterned silicon-on-insulator (SOI) substrates. The Si or Ge NWs grow along <111> directions until they get in contact with the SiO surface where they pursue their growth along <110> directions, parallel and in contact with this surface. This guided growth suddenly kinks if the contact with SiO_x ceases. Growth of InP nanowires along <001> has also been shown to be possible if initiated on a $SrTiO_3$ epitaxial layer deposited on Si (001) (K. Naji, Université de Lyon/ECL, Ecully, France).

T. Xu (IEMN, Lille, France) reported scanning tunneling microscopy investigations performed on Si nanowire sidewalls. The sawtooth side facets systematically show Au-induced reconstructions, Au being the catalyst material.

Impressive realization of organized arrays of InGaN-based nanocolumns obtained by selective area growth on masked surfaces has been achieved by K. Kishino's group (Sophia Nanotechnology Research center, Tokyo, Japan). Development of light emitting diodes fabricated from these nanocolumns is going on rapidly.

M. T. Borgstrom (Lund University, Sweden) has shown that using HCl gas during the vapor phase epitaxy of InP nanowires helps to decouple axial and radial growth. A very selective axial growth has been demonstrated.

It was clearly established that attempts to dope nanowires often result in unexpected effects on the morphology: faceting of the sidewalls for B-doped Si nanowires (F. Li, University of Oxford, UK); increase of volume and density for Mg–doped InN nanowires (T. Gotschke, Research Center Jülich, Germany).

Many presentations focused on the possibility to control the nanowire crystal phase (wurtzite or zinc blende) in compounds semiconductors, or at least to obtain stacking fault-free nanowires. These studies have identified, both experimentally and theoretically, specific conditions meeting such objectives, but it appears that a perfect control remains very challenging. In InAs nanowires, crystal phase transition from wurtzite to zinc blende was observed above a critical diameter (~100 nm) which depends on growth temperature (J. Johansson, Lund University, Sweden). Slower growth rates were shown to be favorable to stabilize the pure wurtzite structure (H. Shtrikman, Weizmann Institute of Science, Israel). It was predicted (and also observed) that zinc blende can be obtained not only at very low supersaturation, but also at very high supersaturation (V. Dubrovskii, St Petersburg Physics and Technology Centre RAS, Russia). Alternatively, the control of periodic arrays of twin boundaries in single-phase has been achieved (R. Algra, Materials Innovation Institute, Delft, The Netherlands).

The workshop ended with an original presentation by E. Gil (LASMEA, Clermont-Ferrand, France) reporting exceptional GaAs nanowire growth rates elaborated by hydride vapor phase epitaxy (40 µm length in 15 min) with long segments (tens of µm) of pure and twin-free cubic structure.

Conclusion

In conclusion, the NWG2009 workshop has provided a forum for presenting the most recent advances on nanowire growth mechanisms, contributing actively to the progress of this challenging topic. Since many nanowire growth issues are still very topical, the NWG workshop has to be maintained. The steering committee has decided that it should continue with a similar format (number of participants limited to about 150 people, about 2 days duration) in 2010. The topics of NWG2010 should keep highly focused on nanowire growth in order to avoid overlapping with other conferences (ICON, MRS meetings, MBE or MOCVD conferences ...), where the applications of nanowires can be presented and discussed in more details.

Acknowledgements

The NWG2009 organization has been sponsored by the French GdR "Nanofils et Nanotubes Semiconducteurs", the Centre de compétence NanoSciences Ile-de-France, Riber SA, and the European Nano-ICT Coordination Action. Their substantial support is acknowledged.

List of relevant research teams in the field of semiconductor nanowires

China

- Peking Univ, Dept Phys, Beijing
- Hong Kong Univ Sci & Technol, Inst Nano Sci & Technol, Hong Kong
- Chinese Acad Sci, Inst Phys, Beijing
- Tsing Hua Univ, Dept Phys, Beijing
- Univ Sci & Technol China, Struct Res Lab, Anhua
- City Univ Hong Kong, COSDAF, Hong Kong

South Korea

- Pohang Univ Sci & Technol, Dept Mat Sci & Technol, Pohang
- Korea Adv Inst Sci & Technol, Dept Chem, Taejon
- Chonbuk Natl Univ, Semicond Phys Res Ctr, Chonju

Japan

- Natl Inst Mat Sci, Adv Mat Lab, Tsukuba, Ibaraki
- Tohoku Univ, Grad Sch Sci, Dept Phys, Sendai, Miyagi
- Hokkaido Univ, RCIQE, Sapporo, Hokkaido
- Osaka Univ, Grad Sch Sci, Dept Phys, Osaka
- Kyoto Univ, Inst Adv Energy, Uji, Kyoto
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- Univ Arkansas, Fayetteville
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- IBM Corp, Div Res, TJ Watson Res Ctr, Yorktown Hts
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- Univ Cambridge, Dept Mat Sci & Met, Cambridge, United Kingdom
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- CEA Grenoble, France
- Ecole Polytech Fed Lausanne, Inst Mat, Lausanne, Switzerland
- Institute for Semiconductor and Solid State Physics, University Linz, Austria

Potential applications of nanowires
Semiconductor families, applications and industrial actors

Popularity of semiconductor families in nanowire research

33 %	ZnO
28 %	Si, SiGe, SiC
17 %	III-Vs (excluding nitrides)
12 %	II-VI (excluding ZnO)
10 %	GaN and other nitride

Fields of nanowire applications

The potential applications which are the most investigated today are:
- Nano-electronics (transistors, spintronics)
- Light emitting devices (LEDs lasers), photodetector
- Photovoltaics
- Field emission
- Biological and chemical sensors
- NEMS and MEMS

Main industrial companies involved in the development of nanowire-based products:
- Samsung
- Hewlett Packard
- Nanosys Inc
- Philips
- IBM
- Sharp
- Qunano AB

Annex II

I. NODE project objectives and main achievements

Overview of the general project objectives

Materials growth and processing technologies of semiconductor nanowire devices were developed and evaluated for their possible impact as key add-on technologies to standard semiconductor fabrication. The goal was also to reach a deepened understanding of the physics of one-dimensional semiconductor materials and nanowire-based devices, and to develop new functionalities not found in traditional higher-dimensional device structures.

NODE studied in detail a set of key device families based on semiconductor nanowires, such as tunneling devices, and field-effect transistors, as well as explored unique opportunities that may be offered by nanowires in areas for storage applications. NODE also made a dedicated effort to evaluate the potential for integration of nanowire-specific processing methods and to assess the compatibility with requirements from conventional semiconductor processing, as well as evaluate novel architectural device concepts and their implementation scenarios. More specifically the main objectives of NODE were:

- To build and evaluate electronic devices based on semiconductor nanowires:

  > NW-based transistors with increased frequency response and decreased power consumption

  > Nanowire logic elements

  > Explore potential for novel device designs using nanowires

- To assess nanowire growth and related nanostructuring in terms of up-scalability and Si-integration potential

Achievements

The research in NODE in many cases represented the state-of-the art in its field. The NODE partners are currently in the research forefront in areas such as (i) understanding of nanowire growth mechanisms, (ii) control of nanowire growth and nanowire doping (iii) characterization of the structural properties of nanowires (iv) processing of vertical nanowires structures (v) device research and development along the two tracks: InAs nanowire wrap-gate FETs and Si nanowire tunnel FETs, using both etched (fully-CMOS compatible) and bottom-up grown nanowires.

Since the project included partners with strong background in research related to CMOS-integration, NODE had a strong focus on finding CMOS-compatible growth methods and processing conditions. Important sub-projects have therefore been to develop growth methods where gold is not required, and catalyst-free techniques have been developed for both InAs- and Si-nanowires, and Al, Pd, Ag seeding of Si nanowires has been demonstrated. A particular effort was also made on investigating the effect of gold on Si nanowires during growth and processing.

Design, fabrication and characterization of the first reported vertical RF-compatible nanowire transistors were carried out, demonstrated with InAs wrap-gate nanowires. Steep slope devices based on Si-nanowires were implemented, where also the first functional Si nanowire tunnel-FETs processed on 200mm wafers on a CMOS platform were demonstrated. Finally, multi-gated Si nanowire Schottky barrier FETs were realized, where an inverter function was demonstrated.

The NODE project has had a very high output in publications, and in total over 100 articles has been published at the end of the project. This clearly shows that considerable progress was made in the project and that the research was competitive on an international level. The NODE partners have applied for at least 48 patents related to nanowire research and development, not including patent applications submitted within the last 18 months that are not yet publicly posted.

2. NODE papers published in refereed journals

Publications 1–94 are already published, 95–96 are accepted for publication, and 97–103 are submitted to refereed journals.

1. “Structural properties of <111> B-oriented III–V nanowires” J. Johansson et al., NATURE MATERIALS 5, 574 (2006)

2. “On the formation of Si nanowires by molecular beam epitaxy” P. Werner et al., INT. J. MAT. RES. 97, 1008 (2006)

3. “Supercurrent reversal in quantum dots” J. A. van Dam et al., NATURE 442, 667 (2006)

4. “Electronic and optical properties of InAs/GaAs nanowire superlattices” Y.M. Niquet, PHYS. REV. B 74, 155304 (2006)

5. “Nanowire-based one dimensional electronics” C. Thelander et al., MATERIALS TODAY 9, 28 (2006)

6. “Position-controlled interconnected InAs nanowire networks” Dick KA, Deppert K, Karlsson LS, et al. NANO LETTERS 6, 2842 (2006)

7. “Optimization of Au-assisted InAs nanowires grown by MOVPE” Dick KA, Deppert K, Samuelson L, et al. JOURNAL OF CRYSTAL GROWTH 297, 326 (2006)

8. “Phase segregation in AlInP shells on GaAs nanowires” Skold N, Wagner JB, Karlsson G, et al. NANO LETTERS 6, 2743 (2006)

9. “Nanowire-based multiple quantum dot memory” Nilsson HA, Thelander C, Froberg LE, et al. APPLIED PHYSICS LETTERS 89, 163101 (2006)

10. "Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor" Lind E, Persson AI, Samuelson L, et al. NANO LETTERS 6, 1842 (2006)

11. "Surface diffusion effects on growth of nanowires by chemical beam epitaxy"Persson AI, Fröberg LE, Jeppesen S, et al. JOURNAL OF APPLIED PHYSICS 101, 1 (2007)

12. "The morphology of axial and branched nanowire heterostructures" Dick KA, Kodambaka S, Reuter MC, et al. NANO LETTERS 7, 1817 (2007)

13. "Sulfur passivation for ohmic contact formation to InAs nanowires" Suyatin DB, Thelander C, Bjork MT, et al. NANOTECHNOLOGY 18, 105307 (2007)

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Graphene grown on SiC by thermal decomposition is at present the most promising candidate for large scale industrial applications requiring high mobility and wafer-scale production. The project involves fabrication of electronic devices from this material and charachterization of graphene on SiC providing a feedback for optimization of the growth material and improving its mobility. The first device application of this project is a Quantum Hall Resistance Standard. Our recent result (Nature Nanotechnology 5, 186, (2010)), obtained in the European collaboration, shows that the Resistance Standard is so far the only practical device where graphene is performing better than conventional semiconductors, taking advantage of large spacing between Landau levels in graphene, in comparison with materials like GaAs. We plan to further develop the first success and produce even better devices by improving the graphene quality and optimizing the device geometry.

The deadline for submitting applications is May 20, 2010

For further information about the position, please contact: **Sergey Kubatkin (kubatkin@chalmers.se)**

⚙ PhD Position (Chalmers University of Technology, Sweden): *"New effects and phenomena in complex metal oxides at the nanoscale"*

Complex metal oxides, based on a perovskite structure, are a particularly interesting group of materials exhibiting a broad spectrum of intrinsic functionalities such as ferroelectricity, high-Tc superconductivity (HTS), colossal magnetoresistance, and multiferroics behavior. Not surprisingly, these compounds are being explored for a variety of new applications. Oxides and strongly correlated electron materials are often considered to be synonyms. Nowadays one has a good understanding of conventional, free electron like materials but, despite several recent breakthroughs, only a rudimentary knowledge exists of the physics behind strongly correlated materials, with their complex ordering phenomena, metal-insulator phase transitions, quantum criticality, relatively low charge carrier density and low dimensionality. Most studies on complex metal oxides have been conducted on thin films or bulk single crystals. However for collective phenomena such as superconductivity, ferromagnetism and ferroelectricity a different degree of ordering is expected to occur near surfaces and interfaces, leading to an intrinsic dependence on the sample size.

The deadline for submitting applications is May 20, 2010

For further information about the position, please contact: **Floriana Lombardi (floriana.lombardi@chalmers.se)**

⚙ Research Faculty Position (Level A/B) (University of Newcastle, Australia): *"MEMS-based nanopositioning systems, power harvesting MEMS devices and MEMS bio-sensors"*

A fixed term Research Faculty position is available within the Laboratory for Dynamics & Control of NanoSystems at the University of Newcastle, Australia. We are seeking a talented and committed individual with the ability to work well in a multi-disciplinary research environment. The areas of interest include: applications of estimation and control in MEMS-based nanopositioning systems, power harvesting MEMS devices and MEMS bio-sensors.

The position is available immediately. The applicants must have a Ph.D. (or be close to completion) in MEMS, Electrical Engineering or a relevant field of engineering or applied physics. They are expected to have a sound analytical background and be able to work in a laboratory environment and on projects that combine high-level theoretical research with experimental investigations. Familiarity with design, prototyping and characterization of MEMS is essential. Knowledge of feedback control systems is highly desirable.

The deadline for submitting applications is May 22, 2010

For further information about the position, please contact: **Reza Moheimani (Reza.Moheimani@newcastle.edu.au)**

⚙ Job openings (Delft University of Technology, Netherlands): *"Biophysics research on nanopores, chromatin and bacteria"*

We are looking for outstanding experimentalists that are eager to participate in our research. Experience in

fields such as biophysics, single-molecule techniques, optical imaging, nanosciences, and molecular or cellular biology, is welcomed. The group aims at research at the highest international level.

The deadline for submitting applications is May 24, 2010

For further information about the position, please contact: **Cees Dekker (c.dekker@tudelft.nl)**

PostDoctoral Position (Graphenea, Spain): *"Chemistry, Physics, and/or Materials Science"*

Graphenea, which is based at the nanoGUNE facilities in San Sebastian, Basque Country (Spain), has been created with the mission of developing graphene-based process and product technology, as well as conducting related research activities. Graphenea will utilize nanoGUNE's state-of-the-art characterization and nanofabrication research infrastructure. The position holder, working closely with Graphenea's scientific director and a technician, will conduct research activities related to graphene synthesis and graphene-based technologies. The position may be renewed annually for up to three years, contingent upon performance. The position requires a PhD in Chemistry, Physics, and/or Materials Science. Candidates should have experience in the preparation of graphene or related materials, with a preferred expertise in the operation of Chemical Vapour Deposition equipment and other deposition techniques. Proficiency in spoken and written English is compulsory; knowledge of Spanish is not a requirement.

The deadline for submitting applications is May 31, 2010

For further information about the position, please contact: **Amaia Zurutuza (a.zurutuza@graphenea.eu)**

PhD Position (Centre Investigacions Nanociencia Nanotecnologia (CSIC-ICN) (CIN2), Spain): *"Quantum Transport in Carbon Nanotubes"*

We are looking for a PhD student with a degree in physics who is eager to do leading edge research in Quantum Transport in Carbon Nanotubes. The research will be focused on the electrical and mechanical properties of structures with dimensions of a few nanometers, such as carbon nanotubes or graphene. These structures are so tiny that quantum effects start to play a dominant role. For e.g. the energy levels are quantized, just like in atoms and molecules. Interestingly, these structures are large and robust enough to be implemented in a variety of different microfabricated devices, which allow the tuning of their quantum properties. This work will be carried within the Quantum Nano-Electronics group, which is part of the Centre Investigacions Nanociencia Nanotecnologia (CSIC-ICN). The group is located at the Campus Universitat Autonoma de Barcelona. The funding for the salaries comes from an EURYI award.

The deadline for submitting applications is June 08, 2010

For further information about the position, please contact: **Adrian Bachtold (adrian.bachtold@cin2.es)**

PhD Position (Instituto de Microelectronica de Madrid IMM-CNM-CSIC, Spain): *"Nano-engineered high performance Thermoelectric Energy Conversion devices"*

A four year position is available for Graduate Students to work towards a PhD Thesis on projects related to the fabrication and characterization of thermoelectric nanowire arrays obtain inside alumina and polymers. The job is funded by a European ERC Starting grant from the European Union. More specifically, the work to be developed by the successful candidate will be related to anodization of aluminium, electrodeposition of thermoelectrics, diblock copolymers, and characterization by raman spectroscopy, electrical, thermal measurements, atomic force microscopy, electron microscopy, x-ray diffraction, etc. The work will be developed at IMM, a consolidate research center for nanoscience. Located at Tres Cantos (Madrid) connected with the city center by public transport.

IMM offers an excellent research environment, with a close interaction with top-level groups working in several areas of Nanoscience

The deadline for submitting applications is June 31, 2010

For further information about the position, please contact: **Marisol Martin Gonzalez (marisol@imm.cnm.csic.es)**

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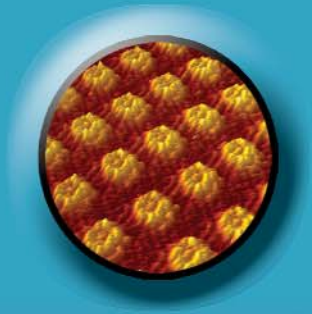
  (Spain, Portugal & France)
- **TNA Energy 2011**
  Trends in NanoApplications
- **PPM 2011**
  Photonics/Plasmonics/Magneto-Optics

SURFACE ANALYSIS

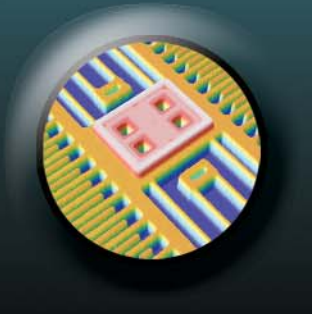


AFM / STM

Materials, polymers, biology, electrochemistry...

SNOM Microscopy

Reflection, transmission, Apertureless...
SECM, Deep Trench, nanopipette probes...



3D Optical Profilometry

New confocal technology...
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