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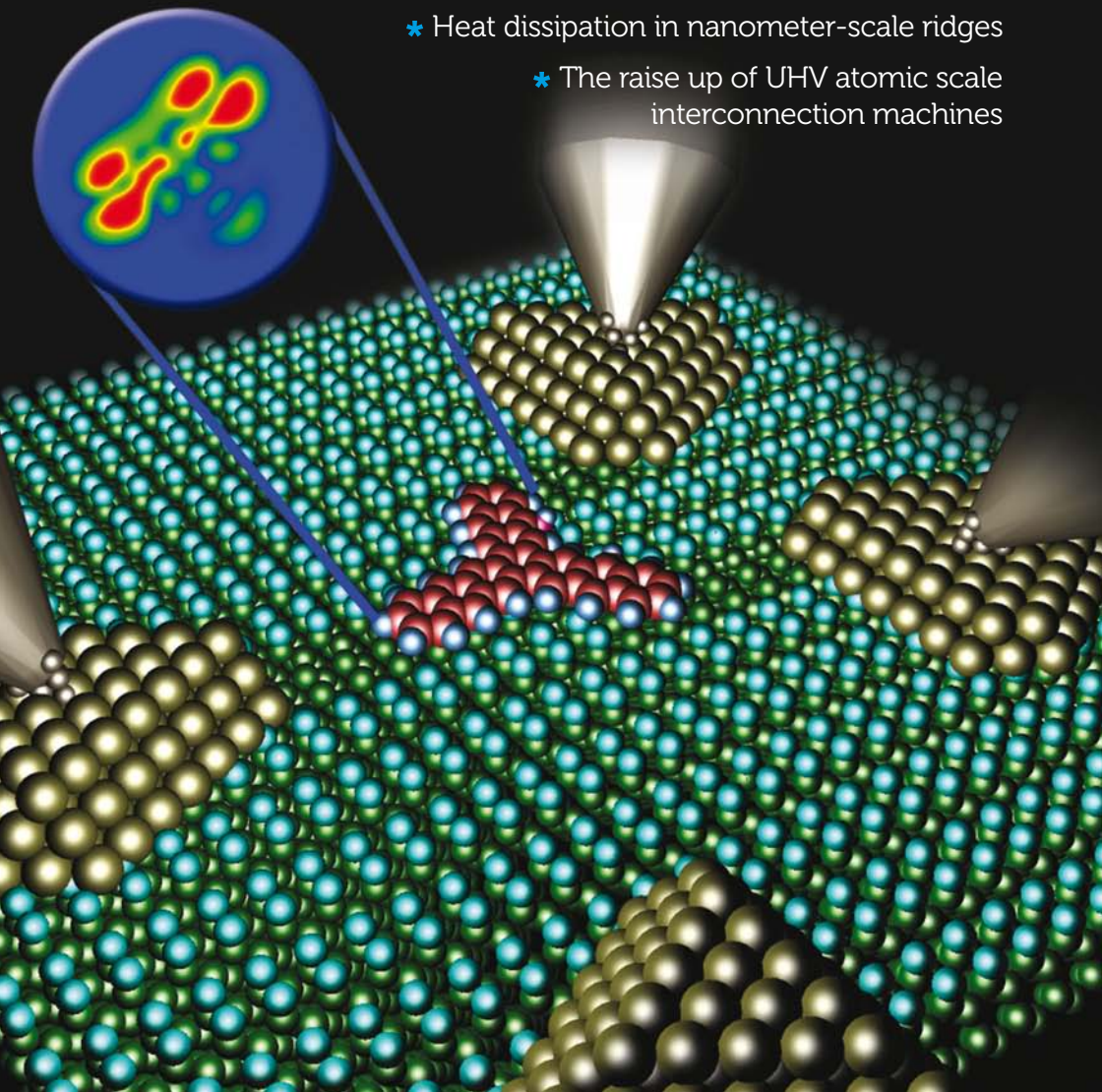
* Atomic Scale and Single Molecule Logic Gate Technologies (AtMol)
* Heat dissipation in nanometer-scale ridges
* The raise up of UHV atomic scale interconnection machines



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dear readers,

This edition contains two articles providing new insights in a relevant field for future nano-electronics applications, i.e. molecular computing at the atomic scale. Since 1974, Molecular electronics had been always associated to the possible future of computers. A new European Integrated Project AtMol was proposed and accepted by the European Commission after the FP7 ICT Call 6 to create this new technology (**www.atmol.eu**). The nanoICT "Mono-Molecular Electronics" Working Group was also set-up in 2008 to reach this objective.

In 2010, the nanoICT project launched its first call for exchange visits for PhD students with the following main objectives: 1. To perform joint work or to be trained in the leading European industrial and academic research institutions; 2. To enhance long-term collaborations within the ERA; 3. To generate high-skilled personnel and to facilitate technology transfer;

The first outcome report ("Heat dissipation in nanometer-scale ridges") of this call investigates experimentally the effect of lateral confinement of acoustic phonons in silicon ridges as a function of the temperature.

We would like to thank all the authors who contributed to this issue as well as the European Commission for the financial support (projects nanoICT No. 216165 and AtMol No. 270028).

> Dr. Antonio Correia Editor - Phantoms Foundation

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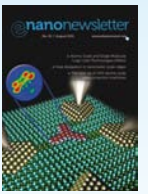

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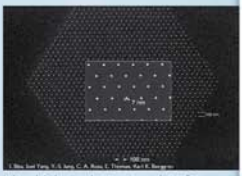

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Atomic Scale and Single Molecule Logic Gate Technologies (**AtMol**) FET ICT Integrated Project (2011-2014)

C. Joachim CEMES-CNRS, France.
AtMol Coordinator

According to the ITRS roadmap, the transistor i.e. the basic switching element of any processor Arithmetic and Logic Unit (ALU) will reach its bottom source – drain distance limit (between 5 nm to 10 nm) in the years 2020's. This will be one limit more after the switching energy problem which started to stop the increase of the computer performance in years 2005-2006. Our global need for more and more computing power in portable and sustainable forms is now pushing the semi-conductor industry to explore new avenues for producing machines to transmit and process information. On the other side of the road, this extreme miniaturisation of the ALU and its associated memory bring again on the table the problem of the limits of the machine in term of size and power consumption whatever the machine: a mechanical machine, a calculator, an emitter… The technical and fundamental limits of machines from the gears to the heat engine, from the relay to the transistor have always been a fantastic playground for physicist and chemists to make progresses in our understanding of the laws of physics.

Since 1974, Molecular electronics had been always associated to the possible future of computers. It is now one of the options among others like quantum computers on the way to bring the next computing technology after our fantastic transistor era. Step by step, Molecular electronics evolves and gives rise to different branches like organic electronics, single molecular devices and molecular logics. Organic electronics had developed its own dedicated technologies like printed electronics. This had not been the case yet for the others branches which remain dependent on very specific fabrication and measurement know-hows like the break junction or LT-UHV STM techniques.

The new European Integrated Project AtMol was proposed and accepted by the European Commission after the FP7 ICT Call 6 to create this new technology for molecular computing at the atomic scale. The members of the AtMol consortium started from the observation that for single molecule electronics to diffuse towards applications and at the same time be used as epistemological devices to explore the limit of calculating machines, it is required to start from the best of surface science. We need to create the ultra clean technology required to construct atomic scale calculating circuits, to interconnect them to the external world and at the same time to invent a proper packaging technology to protect the constructed atomic scale circuit when ready to be extracted from its native UHV environment.

The AtMol molecular chip concept

For AtMol, a molecular chip is a fully packaged and interconnected planar atomic scale complex logic circuit where the ALU is constructed with a set of complex molecule logic gates which may be one day embedded in a single molecule. These are interconnected by surface atomic or molecular wires constructed with atomic precision on a substrate with a large enough surface electronic band gap. The central and entirely new concept to be explore within AtMol is the separation in space of the atomic scale structures of the ALU from the nano/mesoscopic scale interconnects. This new interconnect concept is motivated by the fact that, whatever the architecture of the planar atomic scale complex logic circuit

to be prepared on the surface, there is an incompatibility to deal at the same time and on the same surface with all the interconnection scales from the atomic to the mesoscopic scales (and beyond).

All the known nano-scale fabrication techniques, including e-beam nano-lithography, nano-stencil, nano-imprint, and Focused Ion Beam (FIB), are not atomically clean techniques. For example, in e-beam lithography a resist is used which is very difficult to remove entirely after the nanofabrication step and thus precludes the use of atomically clean surfaces and the associated state-of-the-art surface science characterisation and atomic-scale manipulation tools. Similarly, atoms can diffuse laterally and in a random manner in the nano-stencil technique and when engraving using a FIB. On the other hand, while LT-UHV STM or UHV NC-AFM microscopes are capable of manipulating single atoms, these instruments are not capable of constructing interconnects from the atomic scale (0.1 nm) to the mesoscopic scale (100 nm). A spatial separation of the interconnects between the two faces of a same wafer is the solution proposed by the AtMol consortium. It has the great advantage that the top surface of the wafer is reserved for the planar atomic scale circuit constructions.

The AtMol process flow

AtMol is proposing a comprehensive process flow, spanning the atomic to mesoscopic scale for processing and fabricating a molecular chip.

1) The Atomic scale logic gates and atomic scale circuits are going to be constructed on the front side of the wafer whose atomic scale surface is going to be prepared with care (Fig. 1). Then, the nanoscale to mesoscopic (and, indeed, macroscopic) interconnects will be fabricated on the back side of the same wafer (See Fig. 2). From atomic scale structures of the top surface to mesoscopic connections of the back, solid and rigid nano-vias will be fabricated by piercing, with nanoscale precision, the wafer from the back to the front side. Of course, the piercing is going to be stopped just before the perturbation of the top surface atomic order.

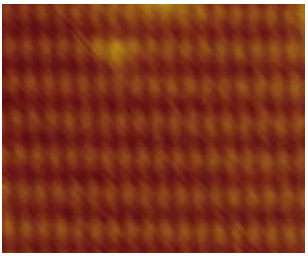

Fig. 1 > An LT UHV STM image (5.8 nm x 6.7 nm) of a Ge(100)H surface carefully prepared by the Krakow AtMol partner. Large terraces of Ge(100)H in Krakow, Si(100)H in Dresden, Nottingham and Singapore, MoS2 in Singapore and AlN in Toulouse AtMol partners are now prepared to become the supporting surface of the AtMol atomic scale interconnects./

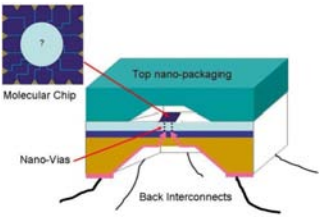

Fig. 2 > The detail configuration of the targeted AtMol molecular chip structure with its back interconnects, its vias through the surface stopped just before disturbing it and its top packaging chip. In this drawing, the top packaging chip is laterally cross cut to help in locating the atomic scale circuit supported by an Si(100)H surface in this case. The insert is presenting this circuit with its 16 Au nano-islands interconnection pads and the location of the active circuit. The question mark is an indication that the exact optimal architecture of this circuit is not yet determined in AtMol (see the main text for the different possible choices). The surface size of the atomic chip is 54 x 54 surface SiH dimers. This is an indication of the simulation target of the Toulouse, Singapore and Barcelona AtMol partners to succeed in associating semi-empirical (N-ESQC) and DFT (TranSiesta) surface transport calculations to predict the best surface atomic scale surface architecture./

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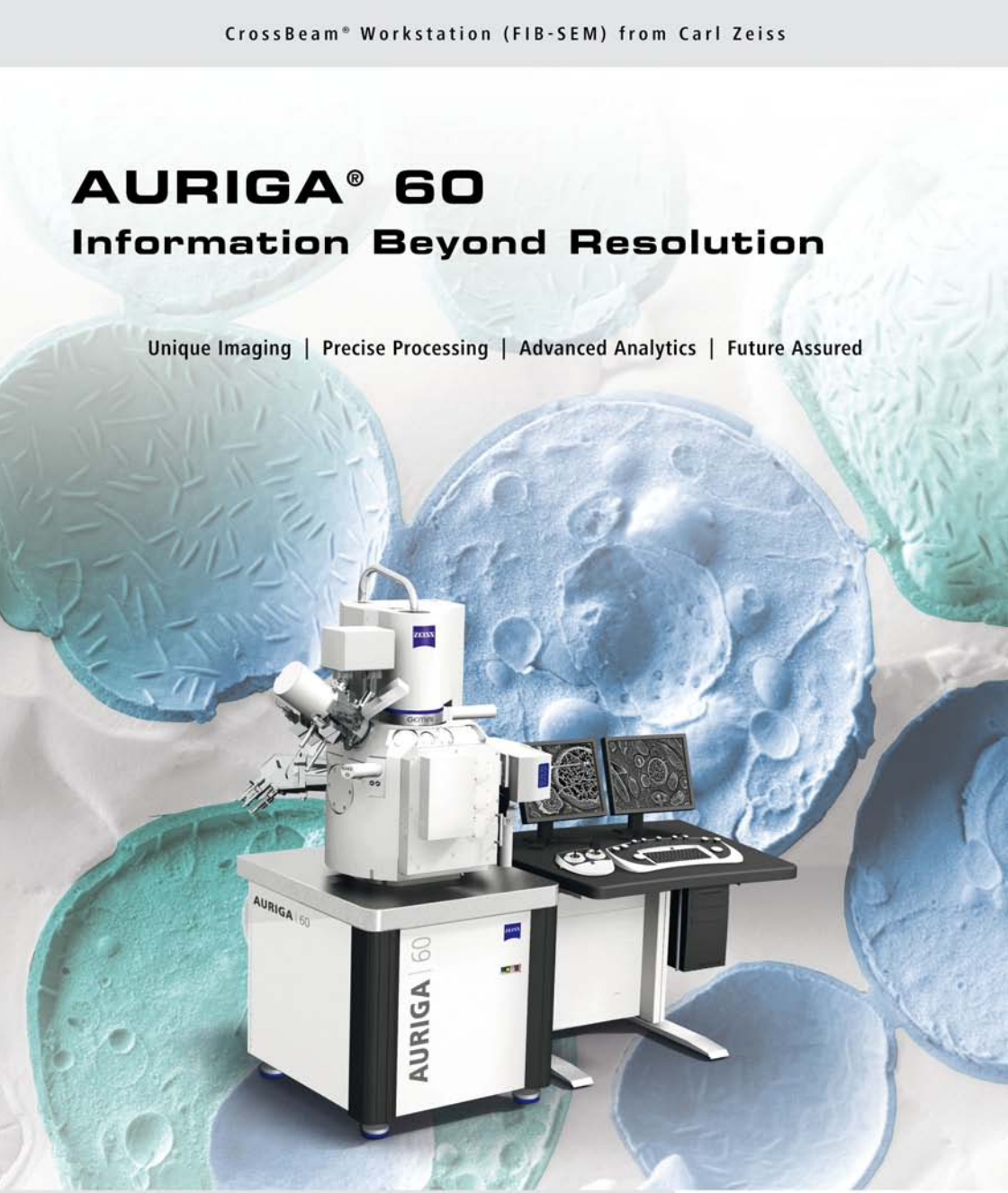

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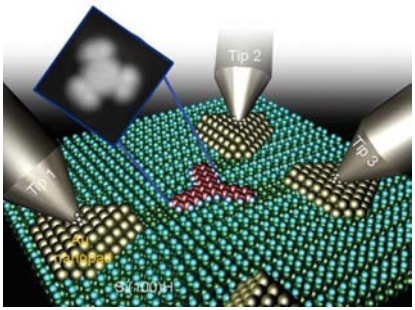

Fig. 3 > A detail atomic scale representation of a top surface contact LT-UHV experiment using multiple STM tips, each one contacting one Au nano-pads. The molecule logic gate represented is here a starphene molecule interconnected in a classical way to 3 quite large surface dangling bond atomic wires, each reaching an Au nano-pad. The 3 AtMol UHV interconnection machines able to perform such multi-probes experiments are discussed in Fig. 4. The insert is presenting the LT-UHV STM image of the starphene electronic ground state obtained by the Singapore and Toulouse AtMol LT-UHV STM. This starphene molecule was synthesized by the Tarragona AtMol partner. Long molecular wires, new molecule logic gates and latching molecules are going to be synthesized by the Berlin, Tarragona and Toulouse AtMol Chemists./

2) The back-side mesoscopic interconnection circuitry and the nano-via through the wafer indicated in Fig. 2 are prepared and UHV cleaned for example before the atomic scale construction step. In this case, the front side is going to be encapsulated using a wafer bonding technique without modifying the back mesoscopic face of the wafer.

3) The top surface planar atomic scale logic circuits will be tested using N probes (see the testing principle presented in Fig. 3) located within a UHV-compatible atomic scale interconnection machine (Fig. 4). These interconnection instruments are integrated within one large UHV system which incorporates a surface preparation chamber, a UHV-transfer printing device, an FIM atomic scale tip preparation device, an LT-UHV-STM (or NC-AFM) microscope, and a N-nanoprobe system under a scanning electron microscope (or an optical for insulating surface) navigation system. Uniquely, AtMol will use and develop further the only N-probe UHV interconnection machines which are currently existing in the world i.e. in Singapore, Krakow and Toulouse (Fig. 4). These machines are the ultimate UHV compatible multi-probe testers reaching the nanoscale precision. Before encapsulating the front side under UHV conditions, electrical characterisation will be carried out in parallel with the electrical testing of the back interconnects.

Fig. 4 > The 3 AtMol UHV atomic scale interconnection machines in construction. The first one is now being tested in Singapore, the second one in Krakow and the third one in Toulouse. Each one has is own specific characteristics. The Singapore one is fully LT and equipped with a UHV transfer printer. The Krakow one is equipped by a hemispherical electron energy analyser (Auger microscope). Both are equipped by the required high resolution (4 nm) UHV-SEM. The Toulouse one is more dedicated towards large electronic gap surfaces which explained this peculiar multi-probes contacting approach based on metallic cantilevers./

4) New atomic scale construction and fabrication techniques will be fully developed without fear of seeing the atomically precise circuits being destroyed by any subsequent mesoscopic scale interconnection fabrication step. The atomic scale fabrication techniques are under development before being incorporated into back interconnected wafers. For example, AtMol will exploit this capability to develop a unique UHV atomic scale transfer printing technique able to integrate nano-scale contacting metallic pads, long molecular wires, active molecule logic gates, and latch molecules on the front (atomically clean) surface (Fig. 5). This will be supported by the objective of improving the construction of long dangling bond atomic wires on a semiconductor surfaces using local forces instead of inelastic electronic effects of the STM.

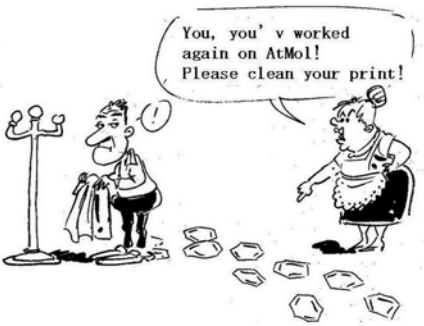

Fig. 5 > A cartoon indicating that the Berlin and Singapore AtMol partners are exploring UHV transfer printing to avoid any nano-lithography steps. Initially developed in Singapore to transfer metallic nano-pads on the Si(100)H surface, the UHV transfer printing technique is now generalized in AtMol to molecular wires and molecule logic gates. This cartoon is also presented here to illustrate how AtMol via its Madrid partner is pro-active in diffusing information to a wide public about AtMol and about the development of Atom Tech in general. This cartoon belongs to a series of 30 drawn by the famous cartoon drawer G. Cousseau invited for the AtMol Kick-off meeting./

Exploring the different molecule logic architectures

At the atomic scale, the main advantage of the AtMol atomic scale chip technology is that it offer a definitive working bench to determine the optimal atomic scale architecture for constructing a complex logic gate able, for example, to add two binary numbers. The fantastic advantage of the front-back side interconnection AtMol innovation described above is that any circuit architecture can be constructed and tested in full planar and UHV technology with an atomic scale technology and with the possibility to determine the exact atomic scale structure of the ALU being constructed. It can be expanded to single molecule mechanics and transmission of mechanical motion.

For “single molecule” molecular logic, the standard solution coming from the 70’s is an hybrid molecular electronics architecture where each molecule in the circuit acts as a switch (or, better, as a transistor). Of course, there are significant problems with this conventional scheme. In particular, it requires a command (for example an electric field or a mechanical push) to be applied on each molecule-switch in the circuit. As a consequence, the distance between each molecule-switch has to be larger than the electron mean free path of the interconnection materials for the electric field to be well defined on each molecule of the circuit. This also requires bringing the command electrodes on many points of the atomic scale circuit. For AtMol, this is not the way to go. But this type of design can be well tested on the AtMol wafer top.

The first AtMol objective is to test semi-classical electronic circuit laws at the atomic scale. Distinct from the well-known Kirchhoff circuit laws, these laws were demonstrated theoretically at the end of the 90s but remain to be experimentally tested. Be it by synthesising specific long molecules having the shape of an electronic circuit or by constructing atom by atom such a circuit at the surface of a passivated semiconductor,

atomic and molecular manipulation and very precise dI/dV spectroscopy using scanning probes (LT-UHV-STM/AFM) are going to provide the definitive experimental testing of those laws. Having verified atomic scale electronic circuit laws, AtMol designer and chemists can generate complete designs of fully integrated ALU atomic scale circuits. More complex semi-classical circuits will be designed theoretically and tested up to the point where the maximum reachable complexity will be attained due, for example, to the output current intensity falling below a minimum detectable threshold.

The second AtMol objective is to determine how the very new Quantum Hamiltonian Computing (QHC) concept introduced in the European Pico-Inside project can reach a larger Boolean logic function complexity as compared with semi-classical atomic scale circuits. In QHC, logic operations are carried out not via charge processing but through quantum information manipulation inside the atomic scale circuit or inside the molecule. In QHC, the electron transfer rate between a drive electrode and an output electrode is controlled by locally changing the Hamiltonian of the molecule (or of the surface atom circuit). In QHC, the decoherence phenomenon is used to build up a measurable output current averaging all the quantum fluctuations. One major architectural innovation is that the inputs are basically classical but locally converted in quantum information (Fig. 6). This conversion is performed by the energy and phase changes of some of the electronic states of the molecule (or of the surface atomic scale circuit). Two strategies will be considered: either the molecule(s) can do everything or a surface atomic scale circuit completed by molecule latches to handle the inputs is preferable to reach large output current (perhaps up to the microampere range).

This design effort will be supported by an intense theory of surface science efforts to take into account for the first time the full electronic contribution of the underneath surface supporting the logic gates. A detail theory of the surface atomic scale structure, its relaxation while contructing surface atomic wire or adsorbing and interconnecting molecule logic gate and molecular wire is going to be developed together with the calculation of the running current (and its associated electronic effects) through the atomic scale surface circuit. New quantum design rules may emerged from those developments which will be immediate feed backed to the AtMol chemists.

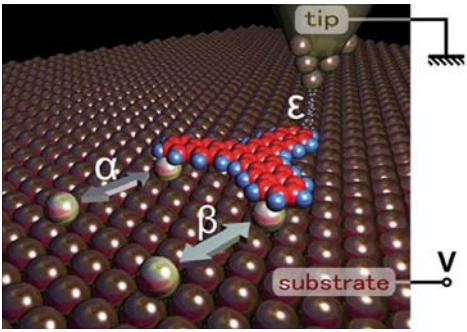

Fig. 6 > The detail atomic scale representation of a LT-UHV STM experiment performed by the Singapore AtMol Partner to demonstrate how the Boolean truth table of a QHC molecule NOR logic gate can be measured. Each Au individual atom is STM manipulated to interact (or not) with one branch of the conjugated starphene molecule. The positioning of an Au atom nearby the molecular branch is a classical input converted in quantum information by the molecule itself. The starphene ground state position is determined by performing an STS spectrum on the output branch of the molecule. The Berlin AtMol partner will perform single molecule pulling experiments to determine the conductance of a single molecular wire (or intramolecular circuit). The Singapore, Barcelona and Toulouse molecule (or surface atomic circuit) AtMol designers are now in full interactions with the Berlin, Tarragona and Toulouse AtMol chemists to create new molecule logic gates and with the Dresden, Nottingham, Krakow and Singapore AtMol surface scientists to create the first surface atomic scale fully interconnected logic gate circuits./

AtMol in 2014

The AtMol consortium members are very committed by the fact that at the same time chemistry, surface science, single atom manipulation, new UHV multi-channel interconnection machines, new UHV printing and packaging techniques need to be developed to construct the first ever single molecule chip. After 2014, AtMol is expecting that its "concept Chip" will be the pivot of the development of real molecular chips and at the same time will point forward the material and technological down limit of a calculator.

To accompany its efforts and to associate more academic and industrial groups to the creation of its new atomic scale technology, AtMol is organizing each 6 months a workshop on topics of high concerns. The 1st AtMol workshop on "Atomic scale interconnection machines" ran in Singapore from the 28th to 29th of June 2011. The 2nd workshop on "Molecular logic architecture at the atomic scale" will be running in Barcelona, January 2012 and the next one on "UHV surface chemistry and UHV transfer printing" in Berlin 6 months after. Output from these workshops (lecture notes, etc.) concerning atomic scale technology will be regrouped in a new series of books entitled "Advances in Atom and Single Molecule Machine" published by Springer.

The AtMol consortium (www.atmol.eu)

CEMES-CNRS (Toulouse)
LETI-CEA (Grenoble)
The Phantoms Foundation (Madrid)
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CIN2 Institute (Barcelona)
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Heat dissipation in nanometer-scale ridges

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Abstract > Heat management in today's electronic devices is critical to prevent possible failures due particularly to cracks. Heat is carried in such devices by electrons in electrical conductors and mainly by acoustic phonons in electrical insulators. We explain the first steps of our work aiming to investigate experimentally the effect of lateral confinement of acoustic phonons in silicon ridges as a function of the temperature. Inspired by the electrical 3ω method, we design a setup that can be used as a mean to generate phonons in ~100 nm wide ridge nanostructures and as a thermometer that allows tracking the generated heat flux.

1. Introduction

Works performed over the last decades have shown that electronic devices with nanometre-scale dimensions are subject to larger temperature-driven stresses in comparison to what had been estimated in the past [1]. In particular, the size of different components of transistors and electronics devices present in printed circuits are now comparable to the key scales associated to electric and heat conduction, namely particles free path and even wavelength in some cases. The case of the heat carriers is particularly of interest because it involves phonons that have free paths estimated to be larger than the device characteristic length in some cases, undergoing fewer collisions as a consequence. The so-called phonon rarefaction effect is then responsible for higher temperature in the heat source than what can be estimated with the usual Fourier-based heat conduction equation [2]. Larger temperature gradients are then responsible for cracks as differential thermal expansion at material interfaces is not manageable.

A key parameter in the improvement of the device design is therefore the understanding of heat conduction in the devices. Here we focus on one way to measure the implications of the particle behaviour (mean free path) of acoustic phonons when they are confined in tiny structures. We propose a method to analyse the heat flux propagation in these structures and show our first efforts towards the efficient use of the designed samples.

2. Heat flux measurements in low-dimensional samples

A. The macroscopic 3ω method

The 3ω method has been developed since the 1980s, in particular by Cahill [3], with the goal of studying the thermal conductivity of planar materials. Thin films have been investigated widely as well as the thermal boundary resistance between the films [4]. It was extended for multilayer materials or particle-based materials [5, 6]. The method is based on the Joule heating of a metallic wire of micrometric size deposited on top of the substrate that "steals" part of the heat

flux generated. As a consequence, the temperature of the wire gives an indication on the ability of the sample to conduct heat. The use of a harmonic current to heat the wire allows the excitation of the temperature higher-order harmonics. If the heating is not too high, only the third harmonic is excited as will be seen in the following. One can write for a current $I = I_0 \cos(\omega t)$ the generated power due to the Joule heating as

$$P(t) = R\, I(t)^2 = \tfrac{1}{2} R\, (1 + \cos(2\omega t))$$

and the total temperature reads including the heating T_{DC} by DC current :

$$T(t) = T_0 + T_{DC} + T_{2\omega} \cos(2\omega t + \varnothing_{2\omega}).$$

The key point now is the dependence of the wire resistivity to temperature, that is linear in first approximation for low heating: $R(T) = R_0 (1+\alpha\, \Delta T)$. Finally, the voltage of the wire can be written as

$$\begin{aligned} U = RI &= R_0 I_0\, [1+\alpha(T_{DC}+T_{2\omega} \cos(2\omega t+\varnothing_{2\omega}))]\, \cos(\omega t) \\ &= R_0 I_0\, [(1+\alpha T_{DC})\, \cos(\omega t)+\tfrac{1}{2}\alpha T_{2\omega} \cos(\omega t-\varnothing_{2\omega}) \\ &\qquad +\tfrac{1}{2}\alpha T_{2\omega} \cos(3\omega t+\varnothing_{2\omega})] \end{aligned}$$

The use of a lock-in amplifier at the third harmonic enables to measure the amplitude and the phase of the third harmonic and thus extract the local temperature. The amplitude is $U_{3\omega} = \tfrac{1}{2}\, \alpha R_0 I_0\, T_{2\omega}$. The frequency range to be used here is generally between 10 and 5000 Hz. Care has to be taken with the wire width and thickness that should be smaller than the thermal diffusion wavelength in order to prevent from a possible nonhomogeneity of the heat generation in the wire.

This experimental part of the work permits only to get a qualitative idea of the material thermal properties or to make an estimate based on comparisons with reference materials the thermal conductivity of which is known. This is not an easy task as a heating device has to be deposited on top of each sample.

If one wants to find the thermal conductivity directly from the sample, a physical model linking the measured temperature and the substrate thermal conductivity has to be found. A 2D cross-section based model has been used extensively over the past 20 years. It is based on frequency sweeps. The slope of the temperature variation gives the thermal conductivity [3]. Some authors have underlined that better models can be used [7, 8]. Usually, the width of the wire is in the micrometric range, which is reached with standard optical lithography in the fabrication process.

B. Implementation at the nanoscale

The case of nanoelectronic devices is very different to the micrometre-scale one. Even if the heating/sensing system that can be used has the same principle, the sizes are much smaller. We fabricated nanostructures where the heater/sensor lies on top of silicon substrates as represented in Fig. 1. The top of a ridge is a wire, either a metal or doped silicon, which acts as a heater and as a thermometer at the same time. The doped-layer structure requires epitaxial growth of doped silicon.

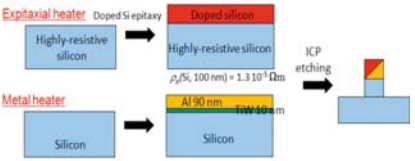

Fig. 1 > Two types of resistive heater for the ridge experiments./

The substrates can be made of high-resistivity silicon. The submicrometer ridges are fabricated with electron beam lithography and ICP dry etching (see Fig. 2, page 14).

This type of structure enables to generate phonons in the ridge and to measure the heat flux flowing to the substrate. An adaptation of the 3ω method is then used to heat the wire and measure the wire temperature. As it has been previously explained, a harmonic electrical current generates the heat at 2ω due to Joule effect and lock-in detection allows measuring the in-phase 3ω voltage

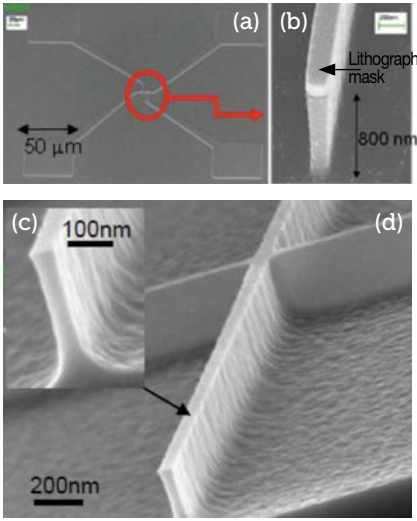

Fig. 2 > Examples of the fabricated structures: (a) Overall view of one layout (b) Zoom on a ridge with a metal wire before mask removal (c) Zoom on a ridge with a doped silicon layer showing a nonrectangular shape after reactive ion etching (d) Connection between the measured wire and electrical access./

component proportional to the wire 2ω temperature. Note that one needs generally to filter the spurious signal generated by the source at 3ω. A 4 points measurement is better usually, but 2 points can be also used in some cases. The difference with the macroscopic method is that a different physical model has to be used to link the wire temperature to the heat flux transmitted to the substrate.

The first test is to measure the electrical resistance of the device as a function of the temperature, as varying this parameter allows determining the value of the temperature coefficient α needed for the measurements. It can be found that α is positive or negative depending on the temperature and the type of heater/sensor. The major experimental difference with the macroscopic method is the value of the resistances that can be as high as 20 kΩ in certain cases. The standard wire method deals in general with a few Ohms.

3. Phonons in silicon and some size effects

A. Silicon properties

Silicon is a semiconductor where electrons are the charge carriers but most of the heat is carried through phonons. The thermal conductivity of pure silicon is $\lambda \approx 149\ Wm^{-1}K^{-1}$ at room temperature, which is high in comparison to amorphous materials such as SiO_2 with thermal conductivities two orders of magnitude below. Note that gold, one of the best metallic heat conductors, is only conducting heat two times better than silicon. Despite this high thermal conductivity, it can be shown with the Wiedemann-Franz law that the electronic contribution to thermal conductivity is negligible even at moderate doping levels. The phononic thermal conductivity of a crystal can be written

$$\lambda = \sum_{pola.} \int_0^{+\infty} \frac{1}{3} \hbar\omega \frac{df}{dT} (v_g \tau)\, g(\omega)\, v_g d\omega$$

where the integration spans over the frequency ω and the discrete sum over the three different polarizations. $\hbar$ is the reduced Planck constant; f is the Bose-Einstein distribution; T the temperature; g is the phononic density of states; v_g the phonon mode group velocity; τ is the phonon relaxation time and (v_g τ) is the phonon mode mean free path. The high thermal conductivity is therefore due to either high velocities, large density of states or large phonons mean free path.

B. Acoustic phonons, mean free paths

In general, mean free paths are parameters that are not very-well known as they (1) depend strongly on the frequency whereas they are generally calculated as an average and (2) are very difficult to measure at room temperature. Some early

measurements were reported in the 1960s at lower temperature [9], and more recent experiments using electrical methods [10] and time-domain thermoreflectance have shown that part of the phonon mean free path distribution should lie at lengths above 500 nm. An alternative way to get insights in the issue of mean free path is the use of molecular dynamics simulation. Henry and Chen [11] recently calculated a distribution of the mean free paths for silicon, finding indeed that around 30% of the thermal conductivity was due to mean free paths larger than 1 micrometer. This is consistent with the estimation [10] that the mean free path should be around 300 nm for silicon. Here one should keep in mind that the widespread evaluation of the mean free path $v_g\tau$ from $\lambda=1/3\ \rho\ c_p\ v_g\ (v_g\tau)$ is delicate in the sense that it counts all the optical modes in the specific heat cp, whereas they are not expected to play a key role in the thermal conductivity due to the flatness of their dispersion relation ($v_g\approx0$). Here ρ is the material density as usual. This approximation underestimates the effect of the phonon rarefaction in small devices. Recent works performed with nanowires [12, 13, 14] and with embedded nanoparticles [15, 16], targeting thermal conductivity reduction in thermoelectric materials, have also highlighted the effect of roughness [14, 15] in addition to the phonon-particle confinement effect. Here we do not discuss the suspended wire issue as it is for the moment less relevant in nanoelectronics.

We need also to underline the role of the interaction of electrons and optical phonons with the acoustic ones [17, 18]. Even if optical phonons do not carry heat significantly they interact with the acoustic ones, therefore impacting the thermal conductivity through the scattering mean free path. Note also that electron scattering with optical phonons is significant, and the heat redistribution to acoustic phonons takes place through optical/acoustic phonons scattering interaction. We refer the reader to the mentioned references from the group of Goodson for the study of such phenomena.

4. Heat conduction in electric tracks and ridges

In electronic devices with deposited metal lines or doped silicon tracks, the electronic path lies on top of planar substrates. Considering a phonon mean free path on the order of 100 nm, we present in Fig. 3 three types of possible devices that consist of a ridge on a planar substrate of the same or different material. For simplification, we start with only similar materials. The left device can be treated with the usual Fourier heat conduction, the middle one is different as even if the nanostructure on top is large and is in a thermal equilibrium the thermal constriction resistance to the cold bath has to be described by a subcontinuum heat conduction. The right device is even further complicated as the size of the structure does not allow an equilibrium inside due to its small size and the fact that phonons are not trapped in the cavity but can also escape. The centre figure is typical of the rarefaction effect [19], when the phonon statistics impinging the constriction is different than the equilibrium one. The right one has been tackled in a theoretical paper [20]. In principle, the Boltzmann transport equation has to be used for calculating the heat flux in structures such as the centre and right ones but approximate methods have been developed such as the ballistic-diffusive equation [21, 22].

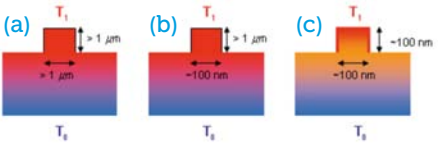

Fig. 3 > Three types of electrical conductors on a planar substrate. The substrate can be either an electric conductor or an insulator. The Fourier description of heat conduction is not adequate for the two last devices (b,c) if the phonon mean free path is of the order of 100 nm or more./

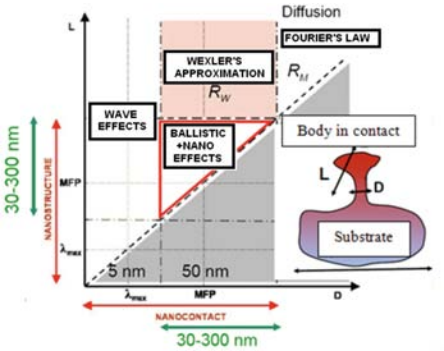

Fig. 4 > Different regimes of heat conduction as a function of the shape of the body in contact with the substrate. Adapted from Ref [20]./

The purpose of our work is to observe these kinds of subcontinuum effects experimentally. We have already measured [23] the expected strong reduction of the thermal conductance in the ballistic regime with respect to Fourier's prediction. Our first results indicate in addition a different behavior than what can be calculated in the purely ballistic case, which is exactly what is pointed out in the analysis developed in Figs. 3 and 4.

Acknowledgements

We thank M. Tilli for providing high ohmic 8" Si wafers. M. Myronov and V. Shah are acknowledged for doing the n+ Si epitaxial growth.

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● **PostDoctoral Position (CEA-Léti, France):** *"Theory and modeling of NEMS based digital functions"*

CMOS technology scaling has enabled significantly reduced energy per operation in integrated circuits. However, these improvements are not in line with the expected performances of future autonomous systems. Autonomous systems that use energy harvesting are attractive for many applications (medical implants, micro-sensors, internet of things devices…). Today technologies used in autonomous systems are not efficient enough for ultra low power applications. The transistor threshold voltage has been scaled to optimally balance leakage and dynamic power but optimized performances are below autonomous systems specifications.

The deadline for submitting applications is October 13, 2011

For further information about the position, please contact:

Hervé Fanet (herve.fanet@cea.fr)

● **PostDoctoral Position (CEA-Léti, France):** *"Characterization of a flexible array of tactile sensors"*

We aim to develop a flexible tactile sensor based on MEMS technology developed at CEA Léti. Three-axis force sensors developed at Léti and already tested for texture measurements will be integrated in an array. The work proposed will include both the integration and characterization of the flexible sensor array.

The deadline for submitting applications is October 13, 2011

For further information about the position, please contact:

Caroline Coutier (caroline.coutier@cea.fr)

● **PhD Position (ICMAB - CSIC, Spain):** *"Functionalisation of surfaces with functional organic molecules for electronic or biological applications"*

We are looking for talented chemists motivated to pursue a PhD in the area of Materials Science. The students will be able to join to a pioneer, dynamic and active group from the Department of NanoScience and Organic Materials (**www.icmab.es/nmmo**). This research group approaches some of the most exciting and challenging fields that a chemist and a materials scientist can explore nowadays — the study of advanced organic functional materials and nanoscopic systems with useful electronic (superconductors, metallic conductors, semiconductors), magnetic (ferromagnets, superparamagnets, single molecule magnets, nanoporous magnets, etc), biological and/or optical properties. We also involved on the development of materials processing techniques, molecular self-assembly and on the preparation of functional nanostructured materials.

The deadline for submitting applications is October 15, 2011

For further information about the position, please contact:

Jaume Veciana (vecianaj@icmab.es)

● **PhD Position (IMM - CSIC, Spain):** *"New paradigms and New Devices based on Nanomechanics"*

The aim of this PhD project is the development of new NEMS devices and new sensing paradigms to achieve the ultimate limits in biological detection based on nanomechanics. Silicon nanowires together carbon nanotubes represent the ultimate limit in the minituarization of nanomechanical resonators. It is expected that these devices can be applied for ultrasensitive mass sensing at the sub-zeptogram level and for mass spectroscopy of single biomolecules. However, the achievement of the optimal performance of these devices requires a detailed understanding of the nanomechanical response and a major development of the optical instrumentation for the detection of the picometer scale vibrations. In this PhD project advanced optical instrumentation

and modeling of the nanomechanical and optical response of the silicon nanowires will be developed. Finite element simulations and analytical models will be developed in order to describe how the static and dynamic response of nanomechanical systems with different geometries behaves when subject to biological adsorption. The final aim will be to establish the potential for weighing single biomolecules and measuring molecular recognition at the level of few events.

The deadline for submitting applications is October 18, 2011

For further information about the position, please contact:

Montserrat Calleja (mcalleja@imm.cnm.csic.es)

- **PostDoctoral Position (ICFO, Spain):** *"Optics and Photonics"*

ICFO – The Institute of Photonic Sciences is a center based in Castelldefels (Barcelona), Spain, devoted to the research and education of the optical and photonic sciences, at the highest international level. No restrictions of citizenship apply to the ICFO post-doctoral contracts. Candidates must hold an internationally-recognized PhD-equivalent degree in a field of science and engineering related to optics and photonics. Suitable backgrounds include optics, physics, mathematics, electronics and telecommunications engineering.

The deadline for submitting applications is October 20, 2011

For further information about the position, please contact:

Ariadna García (ariadnag@heuristica.org)

- **Postdoctoral and PhD positions (University of the Basque Country UPV/EHU, Spain):** *"Dynamical processes in Open Quantum Systems"*

Applications are invited for postdoctoral and PhD positions link to a five year project on the topic of Dynamical processes in open quantum systems as part of an European Research Council Advanced grant (DYNamo project). The project will be conducted between the NanoBio Spectroscopy Group and ETSF Scientific Development Centre in Spain and the Theory group of the Fritz-Haber-Institut in Berlin. The aim of the research project is to develop new concepts for understanding, identifying, and quantifying the different contributions to energy harvesting and storage as well as describing transport mechanisms in natural light harvesting complexes, photovoltaic materials, fluorescent proteins and artificial (nanostructured) devices by means of theories of open quantum systems, non-equilibrium processes and electronic structure.

The deadline for submitting applications is October 31, 2011

For further information about the position, please contact:

Angel Rubio (Angel.Rubio@ehu.es)

- **PostDoctoral Position (CEA-Léti, France):** *"CMOS electro-optical bridge for network-on-chip and optical network"*

The forecasted developments of high-performance computing (HPC) and Cloud computing induce new needs for computation density and data mining. The architectural model is built from a large number of processors sharing a huge memory (eventually several terabytes).

Besides, while networks-on-chip (NoC) are becoming the dominant interconnection paradigm within chips, the connections to large memories are still point-to-point. The gap between the theoretical computing power and the effective or real computing power is hence widening because of bandwidth limitations to shared memory and increasing communication latency.

Emerging high-bandwidth connection standards (DDR3, WideIO…) remain incremental solutions and do not allow concurrent accesses to a large number of memory banks.

The deadline for submitting applications is October 31, 2011

For further information about the position, please contact:

Yvain Thonnart (yvain.thonnart@cea.fr) *

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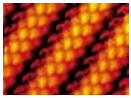
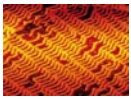
RESEARCH PROGRAMMES

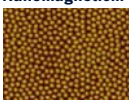
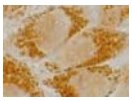
- Molecular nanoscience




- Scanning probe microscopies and surfaces




- Nanomagnetism

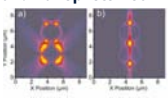



- Nanobiosystems: biomachines and manipulation of macromolecules

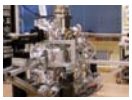

- Nanoelectronics and superconductivity



- Semiconducting nanostructures and nanophotonics




- Nanofabrication and advanced instrumentation

IMDEA-Nanociencia is a private Foundation created by joint initiative of the Comunidad de Madrid and the Ministry of Education of the Government of Spain in February 2007 to manage a new research Institute in Nanoscience and Nanotechnology (IMDEA-Nanociencia). The Institute is located at the campus of the Universidad Autónoma de Madrid in Cantoblanco.

The Institute aims at performing research of excellence in selected areas and offers attractive opportunities to develop a career in science at various levels from Ph.D. students to senior staff positions.

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Nanociencia y Nanotecnología: lo pequeño es diferente
Nanoscience and Nanotechnology: small is different

nanoICT Conf Report

7th International Thin Film Transistor Conference-ITC 2011

3-4 March 2011, Clare College, Cambridge

Organisers

W.I.Milne > Engineering Dept, University of Cambridge, UK.
Arokia Nathan > Electrical & Electronic Engineering University College, London, UK.

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Sponsored by:

The aim of this meeting was to highlight the on-going work on Thin Film Transistors (TFTs), including a-Si:H and related materials systems such as nano, micro and poly crystalline silicon. Sessions however also included work on metal oxides, organics, semiconducting nanowires, carbon nanotubes (CNTs) and naturally the new "material of choice" graphene. Thin-film Transistors (TFTs) have become increasingly important since amorphous silicon (a-Si:H) TFTs were first incorporated in the backplanes in AMLCD TVs. They of course are now being considered for a variety of other applications including RFID tags, sensors, smart tags, etc. and increasingly in flexible electronics. However the electronic properties of a-Si:H limit its possible applications and a variety of different material systems are now being investigated as alternatives.

This year the conference theme was on Novel Materials, Processing and Device-Circuit Integration. There were 110 abstracts submitted and 150 attendees many from the Far East.

There were 17 invited speakers and 29 contributed papers who presented their work on a variety of thin film material systems. There were presentations on CNTs and nanowires for use in TFTs. In terms of distribution, an equal balance in presentations was achieved between materials and applications, fulfilling the primary theme of ITC2011.

Much of the meeting concentrated on the production, characterisation and application of metal oxide based semiconductors although there were also several reports on the use of organic based material systems for TFTs. Metal Oxide transistors are becoming increasingly important as their mobility is much higher than those of amorphous silicon based TFTs and, as their stability is improved, their use in practical systems including flat panel displays, sensors and LEDs cannot be far away.

There were 7 oral sessions and a poster session on both afternoons. The first session was based on Materials & Processing and the invited papers in this session were presented by Hiroshi Tanabe from NEC and Richard Wilson from CDT. Dr Tanabe's presentation was on TFT technologies for Flexible Displays based on the production of metal oxide TFTs at low temperatures using an excimer laser annealing technique. Richard Wilson's talk concentrated on solution processing of organic TFTs with field effect mobilities in excess of 1 cm^2V^{-1} cm^{-2}. The optimisation of the solvent selection from which the material is deposited is key to enhancing and controlling crystalline domain formation.

Session 2 and 8 concentrated on Thin Film Transistors themselves and the invited talks here were given by Kenji Nomura from Tokyo Tech and Elvira Fortunato from FCT-UNL, Portugal. In his presentation Prof Nomura described the work they have been doing to

improve the stability of a-In-Ga-Zn-O TFTs and Prof Fortunato's talk concentrated on transparent electronics with emphasis on the production of both p-type and n-type TFTs. Gilles Horowitz from the Université Denis-Diderot covered the modelling of organic TFTs and Simon Ogier from PeTEC presented their work on backplane technologies for flexible displays.

Novel devices and their applications were described in Session 3. Sigurd Wagner from Princeton reviewed their work on self aligned amorphous silicon transistors and Yue Kuo from Texas A&M described his work on non-volatile memory based devices based on floating gate amorphous silicon TFTs. This was followed by Mutsuku Hatano from Tokyo Tech who gave her vision of the future-integration of wireless-communication functions on Display Panels using TFT technology.

Sessions 4 and 6 looked at TFT circuits and System Integration and involved 4 further invited talks. Prof Takao Someya from Tokyo University gave an excellent presentation on his work on foldable and stretchable electronics using organic based transistors and memories and this was followed by Prof Jin Jang from Kyung Hee University in Korea who presented their research on the stability and flexibility of a-IGZO Transistors on plastic and their application to circuits.

The second session (Session 5) on Materials and Processing was held on the morning of the second day and mostly concentrated on metal oxide materials and devices. Andrew Flewitt from Cambridge University and Thomas Anthopoulos from I.C. were the invited speakers and covered respectively insulators and semiconducting materials deposited at low temperature using a novel sputtering method and spray pyrolysis processed ZnO for use in TFT manufacture.

Session 7 was sponsored by nanoICT EU project and the invited talks were on CNTs for TFTs by Prof Didier Pribat of Sungkyunkwan University in Korea and Circuits based on graphene by Markuu Rouval from the Nokia Research Centre.

74 posters were presented in the two sessions and the banquet was held in Clare College which is the second oldest Cambridge College, having been founded in 1326.

All the sessions were exceedingly well attended despite a tight two-day program with back-to-back talks and posters. Excellent feedback was received from the attendees on the technical quality of the program and the general organization. ITC 2012 will be held in Lisbon, hosted by Uninova, in January 2012.

nanoICT Coordination Action (nanoICT)

www.nanoict.org

The nanoICT plan to strengthen scientific and technological excellence will go beyond the organisation of conferences, workshops, exchange of personnel, WEB site, etc. developing the following activities:

1. Consolidation and visibility of the research community in ICT nanoscale devices
2. Mapping and benchmarking of research at European level, and its comparison with other continents
3. Identification of drivers and measures to assess research in ICT nanoscale devices, and to assess the potential of results to be taken up in industrial research
4. Coordination of research agendas and development of research roadmaps
5. The coordination of national or regional research programmes or activities, with the aim to involve funding authorities in building the ERA around this topic. *

The raise up of UHV atomic scale interconnection machines

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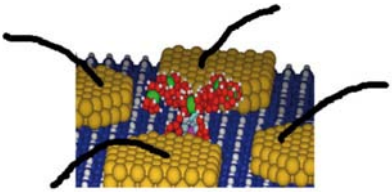

Fig. 1 > A single five wings molecule-motor [1] positioned between a 4 Au nano pads junction constructed at the Si(100)-H surface. The 4 black wires getting out of the surface are indicative of the interconnections step 3 discussed in the text depending on the electronic gap of the supporting surface./

1. Introduction

Single molecule mechanics [1], mono-molecular electronics [2] and surface atomic scale circuits [3] [4] are all requiring a specific surface interconnection technology with an atomic precision and cleanness [5]. In a planar configuration, this surface technology must be able to provide multiple access electronic channels to the atomic (or molecular) scale machinery constructed on a surface (see for example Fig. 1). At the end of the 80's, it was expected that the e-beam nano-lithography technique would be able to provide such a technology [6]. But with its resist based approach, e-beam technique will not face the challenge [7] because it is not able to respect at the same time the atomic scale precision, the cleanness and the expected large number N of access channels to the atomic scale machinery [8]. Alternative nanolithography techniques such as nano-imprint [9] or nano-stencil [10] are neither adapted to encompass all the interconnection stages from the macroscopic to the atomic scale nor clean enough down to the atomic scale. At the turn of the century, this problem triggers a new approach to planar electrical interconnects starting from the bottom that is from the fundamentals of surface science.

In section 2, the general principles of the few UHV atomic scale interconnection machines under test to solve the problem are described. Depending on the electronic gap of the surface where the atomic scale devices and machineries are supposed to work, two families of interconnections machines are being explored. Section 3 is providing one example of an atomic scale interconnection machine designed for the surface of wide gap semi-conductor and insulator materials. Section 4 is giving the example of two interconnection machines for moderate gap semi-conductor surfaces. The design and instrumentation works reported here are the consequence of the EU ICT integrated project Pico-Inside in Krakow and Toulouse together with the A*STAR VIP Atom Tech Phase 2 project in Singapore. It is now further developed in the new EU ICT integrated project AtMol and in the Phase 3 of the A*STAR VIP Atom Tech project in Singapore.

2. Atomically precise electrical interconnection machine

An atomic scale precision, multiple access, electrical interconnection instrument must provide N conducting wires converging toward a very small surface area where an active machinery (see Fig. 1 for a N=4

example) has been constructed with an atomic scale precision. Those N interconnects are positioned somewhere on a large wafer surface. As a consequence, a very efficient navigation system must be designed to locate this very small active area from a macroscopic perspective while keeping the local atomic precision of the interconnection. The solution to this navigation requirement is to combine two types of microscopy: a far field one (optical, scanning electron microscope (SEM)) for large scale navigation and a near field one (Scanning Tunneling Microscope (STM), Atomic Force Microscope (AFM)) for the atomic scale part with a full overlay between those 2 types of microscopy.

An UHV atomic scale interconnection machine is designed to follow a dedicated interconnection protocol. On an atomically clean well-prepared surface, an *atomic scale circuitry* is fabricated (A). To reach a large number N of interconnects and to be able to interconnect each atomic wire to the external world, there is a necessary lateral extension of this circuit to reach N contacting *metallic nanopads* (B) that are positioned around the atomic scale circuit. In the example of Fig. 2, a molecule is connected to these nanopads by *atomic metallic wires.* Depending on the electronic surface gap of the supporting material, the nanopads (B) have to be contacted from the top by a series of N atomically sharp *metallic tips* (C1) or by a series of N *nano-scale wires* (C2) up to the point where mesoscopic metallic wiring or *microelectrodes* (D) can be surface fabricated and contacted by a series of N *micro-scale metallic cantilevers* (E) also from the top of the wafer. During the process, the sequence of those different steps depends on the machine and on the supporting material. What is triggering the choice of the interconnection technology between C1 and C2 (and after the need for the D and E interconnection steps in Fig. 2a) is the electronic gap of the surface that in turn will determine the kind of far field microscopy to be used for navigation over the wafer surface.

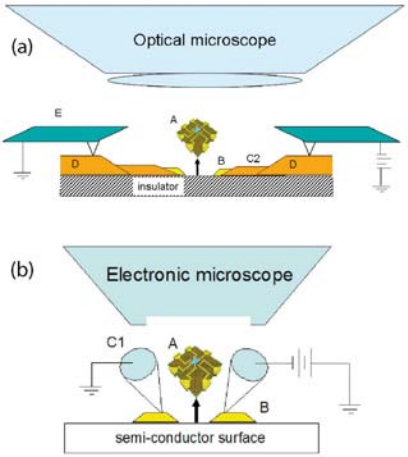

Fig. 2 > Scheme of the atomic scale interconnection machines for (a) wide and (b) moderate surface band gap substrates. A: Atomic scale circuitry, B: Contacting metallic nanopads, C1: Ultrasharp metallic tips, C2: Nanowires, D: Microelectrodes, E: Metallic microcantilevers./

3. UHV interconnection machine for large surface gap

For a large valence-conduction band electronic surface gap (more than a few eV up to 8 eV for standard insulators), SEM is difficult to use as a navigation far field microscope because its electron beam will charge the surface. In this case, an optical microscope is natural candidate for coarse-grained positioning. It determines the minimum length of metallic surface wiring which must be fabricated starting from the nano-pads (B) in Fig. 2a toward the next contact stage based on metallic micro-cantilever. Fortunately enough, with a large surface gap, the surface area of those interconnects can be expanded horizontally without too much lateral leakage current between the different electrodes. This is the basis of the UHV interconnection machine described in this section where a low temperature approach is not compulsory but preferable.

To realize the 5 levels of interconnect described in Fig. 2a in UHV, the deposition of molecules, their observation by NC-AFM and the measurement of their electrical properties, the Toulouse group has designed and constructed a dedicated UHV equipment called DUF (DiNaMo UHV Factory). This equipment allows transferring samples under UHV between five complementary UHV chambers (see Fig. 3):

(1) an MBE growth chamber dedicated to nitride semiconductors growth, metallic nano-pads growth and stencil evaporation for microelectrodes

(2) a room temperature AFM/STM chamber for surface characterization by STM and NC AFM

(3) an AFM/STM chamber modified for nano-stenciling experiments and electrical measurements

(4) a preparation chamber for cleaning substrates, STM tips and AFM cantilevers

(5) a mass spectrometer chamber transformed in a molecular ions source.

For (3) a UHV Omicron Nanotechnology VT STM/AFM head has been modified to accommodate different tools, namely [11]:

1. a flexural-hinge guided (XY) nano-positioner stage (100 µm x 100 µm, repeatability 5 nm) with a closed loop control based on capacitive sensors,
2. an evaporation system highly collimated on the cantilever to perform nano-stencil deposition,
3. a (XYZ) piezo driven table for positioning the metallic micro-combs for the electrical contacts,
4. an optical microscope to control the positioning of the micro-combs.

These modifications were introduced by the mechanical workshop of the Toulouse laboratory. The main advantage of using a commercial UHV AFM/STM is to benefit from the good characteristics for SPM imaging. But the piezo tube used to scan has a range of a few µm only. The addition of a piezo table to move the sample offers the possibility to perform wide range scanning, up to 80 µm SPM images, while keeping the possibility to realize atomic sale imaging with the piezo tube.

One of the disadvantages is the small accessible space around the SPM head. Indeed, it is not possible to place an optical

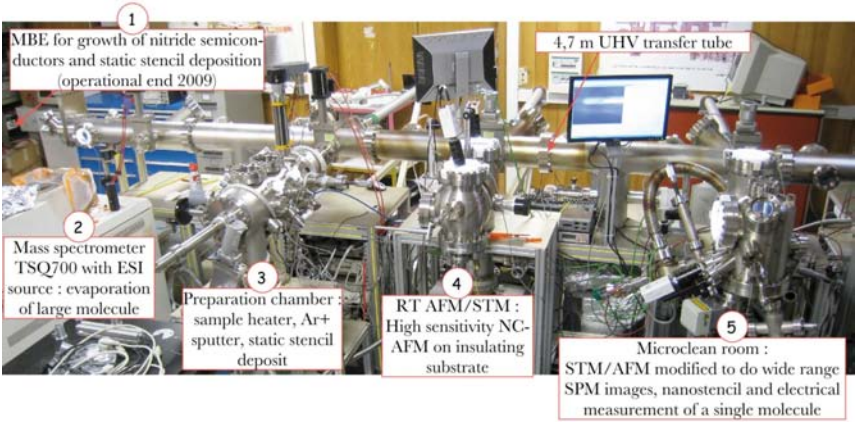

Fig. 3 > The DUF (DiNaMo UHV Factory) equipment allows to transfer samples between 5 complementary UHV chambers in order to realize the 5 levels of interconnect on wide band gap semiconductors (GaN, AlN)./

microscope with normal incidence with respect of the substrate, and an atomic source for the nano-stencil experiments with normal incidence with respect to the AFM cantilever. In our case, the image obtained by the optical microscope comes from a mirror with an angle of 30° with the substrate plane. This gives distorted images, with a loss of resolution: only 3 µm instead of 1 µm in normal incidence. The effusion cell is fixed on a port of the UHV chamber that makes an angle of 33° with the horizontal plane, and another angle of 28° between the two vertical planes passing through the evaporation beam and the central axis of the cantilever. This orientation of the atom beam induces distortion, which should be taken into account in the design of the nano-pattern to be drilled into the pyramidal tip of the cantilever [11].

4. UHV interconnection machine for moderate semi-conductor surface gap

For a moderated valence band-conduction band electronic surface gap (around a few eV), it is not possible to use very long surface metallic circuitry due to the possible lateral surface leakage current between the surface electrodes. In this case, one solution is to use ultra sharp STM like tips positioned from the top on the surface as microelectrodes (Fig. 2b). In this case, the core of the tips will not be in contact with the supporting surface and one can go continuously from a tip apex radius of curvature of a few nanometer up to a 100 microns or more section for the tip body. In this case, navigation on the surface can be performed using an UHV-SEM (Fig. 2b) by grounding the sample during the SEM imaging to avoid the surface charging effect. This is the basics of the UHV interconnection machines described here. A low temperature approach is compulsory with those systems because of the low electronic gap at the surface of the supporting material.

There are two apparatuses that realize the above described design, one is housed in Krakow and the other in Singapore. The Krakow's system consists of three basic segments: multi-probe, low-temperature scanning probe microscope (LT-SPM) and preparation chambers. Multi-probe segment is composed of 4-probe scanning tunnelling microscope (STM) combined with high resolution scanning electron microscope (HR-SEM) and hemispherical electron energy analyser (scanning Auger microscope, SAM) (see Fig. 4). The Auger microscope part is the element not present in Singapore's setups. Composition of the multi-probe segment allows surface element analysis, imaging and measurements of nanostructures conductance with very high-resolution. In accord with the Fig. 2b principle, HR-SEM may act as a navigation to precisely position each of the 4 STM tips

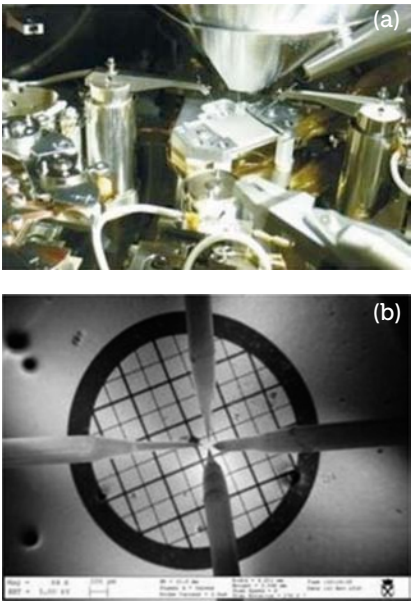

Fig. 4 > (a) View on sample stage of 4-probe microscope; in upper part one can see SEM column and next to it an entrance to hemispherical electron energy analyser; below SEM column there are three of four STM probes. (b) SEM image of four STM probes./

that will be used as microelectrodes. First measurements of conductance of gold nanostructures on Ge(001) surface are in progress.

Next, LT-SPM segment consist of scanning probe microscope that may work both as STM and NC-AFM in a range of temperatures from 4K up to room temperature. Thanks to use of scanner and sample holder embedded in a cryostat, the LT-UHV STM allows for a very high resolution imaging, as well as, stable spectroscopic measurements and atomic scale manipulations.

Furthermore, NC-AFM mode is based on q-sensor device (tuning fork) that enables imaging of conducting, semiconducting and insulating samples at low temperatures (see Fig. 5) and, if required, also simultaneous measurements of tunnelling current. This option makes the Krakow's system a very powerful tool. Last but not least, is the preparation segment that consist of typical preparation equipment such as a XYZ manipulator with electric contact allowing for resistive heating up to 1000K (using a direct heating mode 1200K may be achieved), furthermore the manipulator allows for cooling the sample down to 100K with nitrogen vapour, an ion gun, a low energy electron diffraction system for quick sample quality tests and several ports allowing for incorporation of additional elements (for instance effusion cells or quartz microbalance thickness monitor) into the chamber. All segments are composed of the highest quality elements all of them being compatible to work in UHV environment (less than 3×10^{-10}mbar), and thus allowing for conducting very complex experiments in a single set-up in a very controlled way, starting from sophisticated sample preparation and ending with extensive and complete characterisation.

As the Auger microscopic part of the Krakow's nano-probe instrument is not present in the other setups (see above and below) its potential is briefly described in the following. In Fig. 6, the STM, HR-SEM and

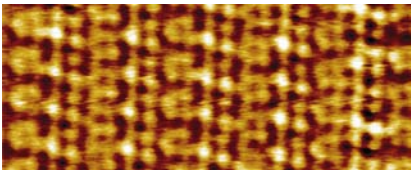

Fig. 5 > InSb surface imaged with q-sensor NC-AFM in temperature 4K./

SAM images of metallic nano-mesa grown on semiconductor substrate are shown. The Ag/Ge(111) is an example of a system for which depending on the deposition conditions, on the successive thermal annealing and on the amount of deposited material the resulting overlayer morphology can be switched from an atomically smooth to a columnar-like [12]. Sample is prepared in the following way: silver in amount of nominal 5 ML is deposited on the germanium surface kept at low temperature. Low energy electron diffraction studies performed immediately after deposition reveal that compact silver film is crated. Such a conclusion follows from the fact that reflections characteristic for the unreconstructed Ag(111) overlayer are observed exclusively on LEED image. One may assume it is a clear and direct indication that Ge substrate is completely buried. In the next step the sample is annealed to room temperature. After annealing a massive

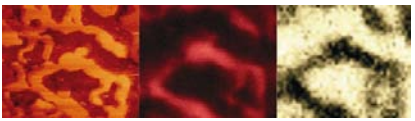

Fig. 6 > STM, HR-SEM and SAM images of the Ag/Ge(111) sample. Image size: 220nm × 270nm. Left panel: STM image; Middle panel: HR-SEM image; Right panel: SAM image. STM image reveals bright nanostructures 2.5nm high. The same regions are marked red in HR-SEM image. In SAM image those structures are black. SAM image was taken for Ge line (E=1144 eV), thus exposing as bright regions containing Ge. Therefore, it is possible to identify the black structures in SAM image (bright and red regions on STM and HR-SEM images, respectively) as silver islands./

morphological reorganization of the Ag film is observed that leads to formation of metallic islands. Left panel in Fig. 6 contains STM image of the Ag/Ge(111) sample annealed to room temperature. As clearly seen, the Ag continuous film has been converted into a network of "nano-mesa" of 10 ML height with atomically flat tops and extended pits exposing the underlying wetting layer (bright and dark structures on left panel in Fig. 6, respectively). The atomic steps bounding the edges are developing into considerably elongated ridges, and appear to be predominantly oriented along the threefold symmetry of the (111) substrate as proved by the HR-SEM analysis.

To further confirm metallic composition of the observed topographic structures Auger spectroscopy in scanning mode is performed. The corresponding Scanning Auger Microscopy images were taken at the Ge line (E = 1144 eV) and Ag line (E = 352 eV). A strong signal contrast in the Ge-SAM image (Fig. 6, right panel) is observed. It clearly indicates the metallic composition of the nanomesa against the semiconductor substrate. Bright regions on right panel in Fig. 6, reveal a germanium content, whereas black regions prove lack of the germanium. Those black regions nicely correspond to red structures seen in HR-SEM image (Fig. 6, middle panel) and to bright regions in SEM image (Fig. 6, left panel). Thus analysis with Auger spectroscopy strengthens the conclusion that observed nanostructures are truly silver nanomesa. Furthermore, in the image, the Ag ridges of the width as low as 20 nm can be resolved providing the capability of high lateral resolution of our Auger microscope based on the Gemini electron column. Here it is worth noting, that in the Ag-SAM image (not shown), together with the high lateral resolution a lower contrast of the Auger signal is observed. The reason for that is

the composition of the wetting layer which is actually the intermixed layer of Ag and Ge.

Following the Fig. 2b principle, the Singapore system consists of five UHV chambers interconnected in a star configuration. A first chamber is dedicated to the surface wafer preparation. A second one is dedicated to metallic nano-islands deposition and transfer (when necessary). A third chamber is equipped with a LT-UHV STM for fabricating the atomic wires, manipulating the molecule logic gate and positioning the metallic nano-islands, one on each termination of an atomic wire. The fourth chamber is equipped with a very efficient UHV-SEM with a resolution better than 5 nm to be able to image the contacting metallic nano-islands and to position a tip apex on each of these nano-islands. Finally, a lateral chamber is dedicated to the UHV tip preparation, sharpening and cleaning. The details of the IMRE Singapore interconnection machine are presented in Fig. 7.

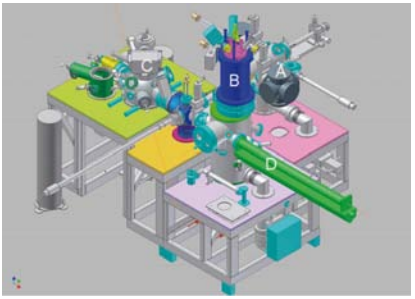

Fig. 7 > The final IMRE Singapore interconnection machine designed in Singapore and constructed by Omicron in 2010. Five main UHV chambers: (A) The preparation chamber with the FIM tip preparation chamber, (B) the LT-UHV-STM from Omicron Nanotechnology and (C) the nano-probe system from Omicron Nanotechnology with its UHV-SEM (3 nm resolution) and the 4 integrated STM. (D) is the delicate LT transfer from the LT-UHV-STM to the UHV-SEM. The UHV transfer print chamber is behind the LT-UHV-STM chamber B./

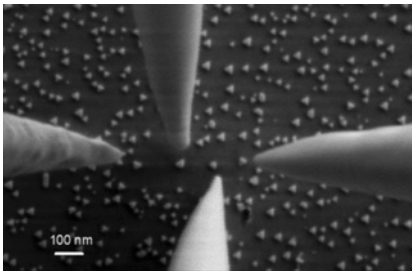

Fig. 8 > SEM image of the tip apex of 4 chemically etched tungsten tips converging toward 4 Au nano-islands which have been manipulated one by one to enable a 4 points like surface conductance measurement. This image has been recorded on a multi-probe system from Zyvex./

Under the UHV-SEM, each nano-island of a contacting nanostructure can be electrically contacted from the top using one ultra-sharp tip per nano-island. Each tip apex is positioned using the UHV-SEM for a precise navigation. The soft contact between a nano-island and its tip apex is controlled by the feedback loop system of an STM meaning that there is one STM control electronic per tip. A SEM image of the contact preparation of 4 nano-islands manipulated on purpose in a row on a MoS_2 surface is presented in Fig. 8 together where the 4 tip apex approaching for the contact are also imaged. Electrical measurements are now in progress to first record the "nano-pad – MoS_2 surface – nano-pad" I-V characteristics for an inter nano-pad distance lower than 10 nm. Then, metallic nano-islands will be transfer printed on Si(100)H surface for surface atomic wire conductance measurements.

5. Conclusion

Connecting the atomic (or molecular) scale machinery to the outer world respecting the atomic scale precision of the construted machinery is a very challenging and complex task. Each of the three described atomic scale interconnection machines housed in Toulouse, Krakow and Singapore possess potential to meet requirements and demands arising upon realization of such a connection [13]. Furthermore, experience and knowledge gained by Krakow's and Toulouse's groups through EU ICT integrated project Pico-Inside and by Singapore's group in parallel through A *STAR VIP Atom Tech Phase 2 set a very fortunate starting point for that quest which is now in full development in the new ICT integrated project AtMol (**www.atmol.eu**).

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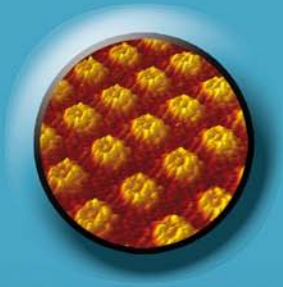

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